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Area efficient digital logic NOT gate using single electron box (SEB)

Davoud Bahrepour*

Mashhad Branch, Islamic Azad University, Mashhad, Iran

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Abstract – The continuing scaling down of complementary metal oxide semiconductor (CMOS) has led researchers to build new devices with nano dimensions, whose behavior will be interpreted based on quantum mechanics. Single-electron devices (SEDs) are promising candidates for future VLSI applications, due to their ultra small dimensions and lower power consumption. In most SED based digital logic designs, a single gate is introduced and its performance discussed. While in the SED based circuits the fan out of designed gate circuit should be considered and measured. In the other words, cascaded SED based designs must work properly so that the next stage(s) should be driven by the previous stage. In this paper, previously NOT gate based on single electron box (SEB) which is an important structure in SED technology, is reviewed in order to obtain correct operation in series connections. The correct operation of the NOT gate is investigated in a buffer circuit which uses two connected NOT gate in series. Then, for achieving better performance the designed buffer circuit is improved by the use of scaling process.

Key words: Digital logic NOT gate, Single-electron devices (SEDs), Fan out, Switching speed, Bit error rate, Single electron box (SEB).

1 Introduction

Continuous improvement in CMOS technology sizes into a nanometer range results in many limitations due to more sub-threshold leakage, gate oxide leakage, and performance. The single-electron devices are among the most promising future devices for its low power dissipation and high density and are attractive candidate for post-CMOS electronics [1–4].

Tunneling of an electron through an insulator is possible in quantum mechanics. An electron tunnels through the insulator if the distance between the conductors is small enough [5–9]. The theory of single electron phenomena shows that the charging energy is:

$$E_c = e^2/C \quad (1)$$

where C is the capacitance of the island. When the island size becomes comparable with the de Broglie wavelength of the electrons inside the island, their energy quantization becomes substantial [8].

In this case, the energy scale of the charging effects is given by a more general notion, the electron addition energy E_a. Most of the time, E_a may be well approximated by equation (2).

$$E_a = E_c + E_k \quad (2)$$

which E_k is the quantum kinetic energy of the added electron; for a degenerate electron gas $E_k = 1/g(\varepsilon F)V$, where V is the island volume and $g(\varepsilon F)$ is the density of states on the Fermi surface [8].

Although SED utilized in many digital logic gates [10–16], the gate characteristics are usually limited to single gate operation and not operation in complicated designs. Some of the most used SEDs are the single electron box (SEB) and the single electron transistor (SET). Figure 1a shows a SEB that operates as a digital logic NOT gate [16] and Figure 1b demonstrates its operation. As shown, SEB consists of a single tunnel junction C_t and one "normal" (non tunneling) capacitor C_b. Between the tunnel junction and normal capacitor, an island is created. It accepts one input, V_i, and produces one output, V_o. Figure 2a illustrates connecting two introduced NOT gate in order to achieve a buffer circuit as an application for a NOT gate. In many cases designers propose a circuit and evaluate them by simulation software. While after introducing

*e-mail: bahrepour@ieee.org

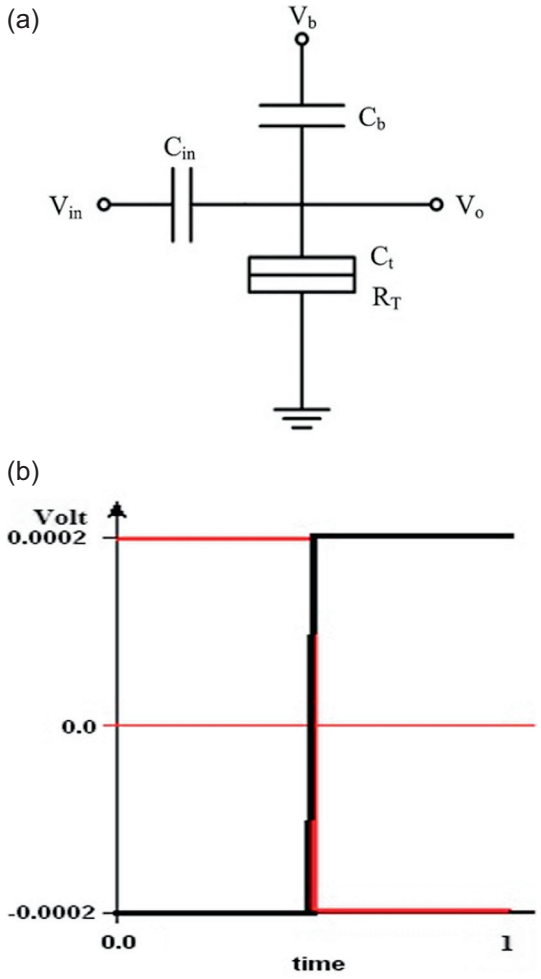

Figure 1. (a) A single electron box which is also a simple NOT gate. (b) Applied input and resulted output displayed in black and red colors respectively.

a digital application for a SED based circuit design optimization is the next challenge [17]. In the following section, the previously proposed SEB based NOT gate is optimized.

In order to have a valid comparison between the performances of two different designs, the first important factor is that the two designs must be implemented in the same technology. In other words, comparison of two designs, which are implemented in two different technologies, is not valid unless the two designs are scaled into a single technology. Therefore, we need an index for SED technology. Index technology enables designers to present different designs in the same technology.

2 Optimizing digital logic NOT gate

This paper aims to optimize the previously introduced SEB based NOT gate (Figure 1a). It is noteworthy that two different designs should be implemented in the same technology in order to achieve a valid comparison. In the other words, comparison of two SEB designs, which are implemented in two different technologies, is not valid unless the two circuits

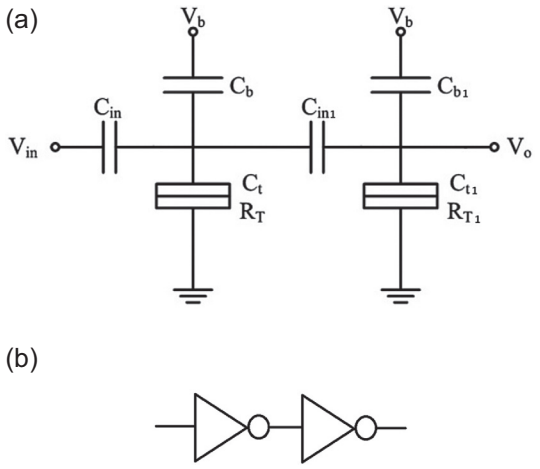

Figure 2. (a) Cascading two NOT gate circuits based on a SEB in order to obtain a buffer gate. (b) gate level design of a buffer using two cascaded NOT gate.

are scaled into a single technology. Therefore, we need an index for SED technology [17].

Any technology index must be based on real technological limitations and it has also a direct relation with the performance of the circuits. One of the well-known technology indices is the minimum feature size for MOSFET technology. This index demonstrates the most important limitations of the technology in an appropriate manner due the fact that it has a clear relation with MOSFET circuit performances. For SED based circuits and regarding the two technology index specifications [17], the total capacitor of the island, C_T, and the tunneling resistor, R_T, are introduced as a technology index. C_T includes the possibility of miniaturization and R_T defines the technology's manufacturing tolerance. Scaling process is a method for achieving better performance in SED based circuits. This method changes the voltage, resistance and capacitance values and leads to better switching speed. However, it does not change the logic function. As mentioned for achieving better performance, NOT gate circuit design is improved by the use of scaling process [17]. The scaling process needs two main parameters named scaling factors. The scaling factors are:

$$\mathrm{CSF} \triangleq \frac{C_{\mathrm{T,new}}}{C_{\mathrm{T,old}}} \tag{3}$$

$$\mathrm{RSF} \triangleq \frac{R_{\mathrm{T,new}}}{R_{\mathrm{T,old}}} \tag{4}$$

where CSF is the capacitance scaling factor, $C_{\mathrm{T,new}}$ is the total capacitor in the new technology, $C_{\mathrm{T,old}}$ is the total capacitor in the old technology, RSF is the tunneling resistance factor, $R_{\mathrm{T,new}}$ is the tunneling resistance in the new technology, and $R_{\mathrm{T,old}}$ is the tunneling resistance in the old technology.

For a logic circuit design consists of more than one island or tunnel junction, the total capacitance for each island and the tunneling resistance for each tunnel junction should be considered, and then the smallest total capacitance and the smallest

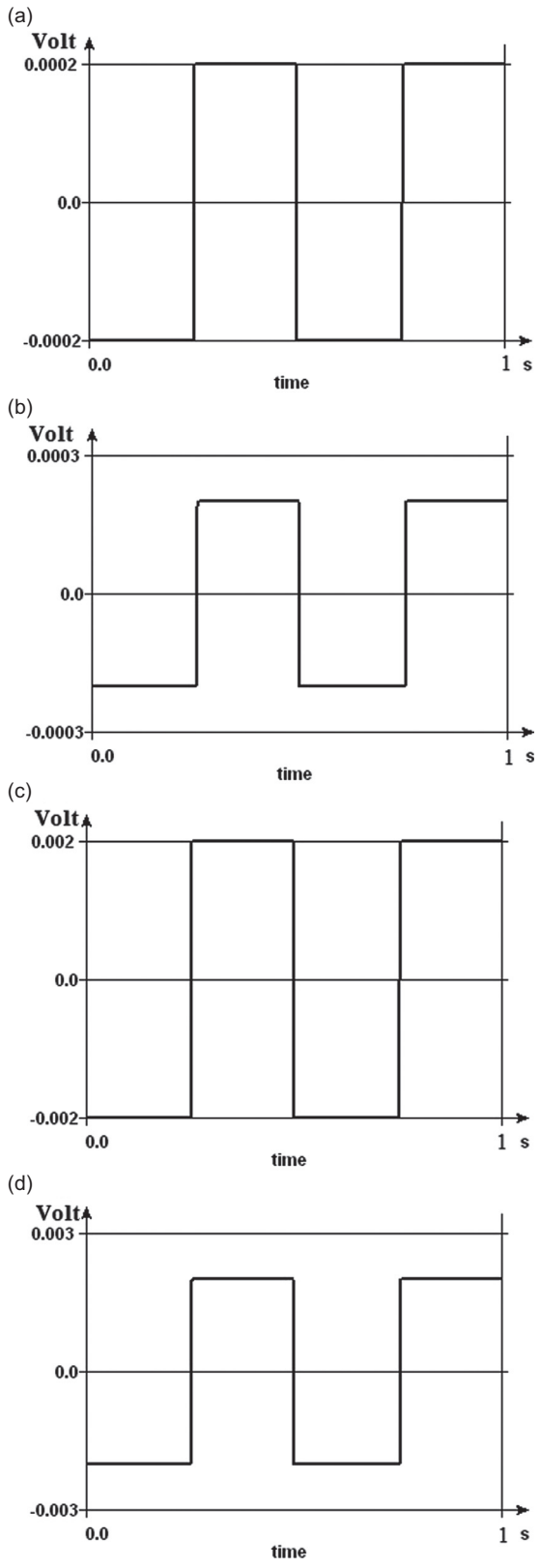

Figure 3. Original SEB buffer design (a) applied input and (b) resulted output. (c) Applied input for the scaled SEB buffer design (d) resulted output.

Table 1. Capacitance values utilized for simulation.

	Original design (aF)	Scaled design (aF)
C_{in}	4	0.4
C_{in1}	2	0.2
C_b	4	0.4
C_{b1}	4	0.4
C_t	392	39.2
C_{t1}	392	39.2
C_T	400	40

tunneling resistance should be selected as the technology of that design.

Here, the mentioned NOT gate (Figure 1) is scaled regard to achieving better performance. As reported in the original paper [16] the total capacitor in the original (old) technology, C_T, and the tunneling resistance in the original (old) technology, R_T, for the NOT gate is 400 aF, and 100 KΩ, respectively. In following, for the new design, C_T and R_T are set to 40 aF and 10 KΩ, respectively. Hence, from equations (3) and (4) both the CSF and RSF are equal to 0.1.

Now by determining the CSF and RSF values for scaling capacitors and the tunneling resistors are multiplied by CSF and RSF, respectively, and the voltages are divided by CSF. As mentioned using scaling process does not change the logic function. utilizing scaling process lead to better performance for a NOT gate and using two NOT gates in buffer design result in an optimized buffer design.

Figures 3 demonstrates simulation results for original and scaled buffer designs. The bias voltage (V_b) is adjusted to 20 mV and 200 mV for original and scaled design, respectively. Also, the tunneling resistance for both designs is adjusted to 100 KΩ. It shows that the tunneling resistance does not change the logic. Table 1 shows the other simulation parameters used in the simulation process.

In this paper, we scaled the capacitors 10 times smaller and the voltage 10 times larger in comparison with the original design. Smaller capacitors lead to the smaller area in the fabrication process and voltage for the area is traded.

3 Conclusion

In this paper, a previously introduced SEB based NOT gate is used to design a buffer gate. It shows that the NOT gate can operate in a concatenated circuit correctly. The main issue for comparing two different circuits is scaling in the same technology. The technology index for SEB based circuit is the total capacitor of the island. Then by introducing the capacitance scaling factor, CSF, and the resistance scaling factor, RSF, the NOT gate and also the buffer circuit is scaled in order to achieve better performance. In the scaling process, the logic function remains unchanged while switching speed obtain. Simulations carried out in commonly used simulators in nano-electronics, SIMON, validate the correct working of these digital functions.

4 Implication and influences

The published work has an impact in providing and introducing a technology index in SED based circuits. This index helps designers to design their circuits and compare them correctly. in this paper by using technology index and scaling process a high performance digital logic NOT gate is proposed based on SEB, however, it can be used in more complex gate circuits such as AND, OR, and XOR.

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