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Current source converter based D-STATCOM for voltage sag mitigation

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Abstract – This paper presents a novel method of realizing one of the custom power controllers, the distribution static synchronous compensator (D-STATCOM) using current source converter (CSC) topology. Almost all the custom power controllers such as dynamic voltage restorer (DVR), unified power quality conditioner (UPQC) including D-STATCOM are generally designed and implemented by using voltage source converters (VSC) and not much research publications with CSC based approach has been reported over the last one decade. Since the D-STATCOM is a current injection device, its performance can be improved when realized by a current-source converter which can generate a controllable current directly at its output terminals and offers many advantageous features. In this paper, an attempt has been made to study the performance of a CSC based D-STATCOM suitable for use in the power distribution system in order to mitigate voltage sag and improve power quality. The proposed model uses a three leg CSC whose switching strategy is based on sinusoidal pulse width modulation (SPWM). The model has been simulated in the Matlab/Simulink environment. The results of the simulation runs under steady state and dynamic load perturbation provide excellent voltage and current waveforms that support the justification of the proposed model.

Key words: Current source converter, Custom power controller, Distribution static synchronous compensator, Proportional integral, Sinusoidal pulse width modulation.

1 Introduction

The emergence deregulated power system operation coupled with the increasing applications of power electronics technology in power transmission and distribution system has led to the research and development of new engineering systems capable of solving various types of power quality problems. The power electronics plays a vital role in FACTS and custom power (CP) devices [1, 2]. The quality of electrical power which is supplied to the customers can be judged in terms of constant voltage magnitude i.e., no voltage sags or swell, constant frequency, constant power factor, balanced phases, sinusoidal waveform i.e., no harmonic content, lack of interruptions and capability to withstand faults and to recover quickly [3]. The VSC topology has been using as the basic building block of the new generation of power electronics controllers emerging from FACTS and custom power research due to the following reasons:

(a) The CSC topology is more complex than a VSC topology in both power and control circuits. Filter capacitors are used at the ac terminals of a CSC to improve the quality of the output ac current waveforms. This adds to the overall cost of the converter. Furthermore, filter capacitors resonate with the ac-side inductances. As a result, some of the harmonic components present in the output current might be amplified, causing high harmonic distortion in the ac-side current. Besides, conventional bi-level switching scheme cannot be used in CSC.
(b) Unless a switch of sufficient reverse voltage withstanding capability such as Gate-Turn-Off (GTO) thyristor is used, a diode has to be placed in series with each of the switches in CSC. This almost doubles the conduction losses compared with the case of VSC.

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(c) The dc-side energy-storage element in CSC topology is an inductor, whereas that in VSC topology is a capacitor. The power loss of an inductor is expected to be larger than that of a capacitor because of the need to store energy by circulating current in inductors which are more lossy than capacitive energy storage [4]. Thus, the efficiency of a CSC is expected to be lower than that of a VSC [5].

However, recent advancement in power semiconductor switching devices and control strategies of CSC topology may overcome the drawbacks mentioned above in the near future because of the following reasons:

(i) The CSC is usually more reliable and fault tolerant than a VSC due to the presence of large series inductor which limits the rate of rise of current in the event of a fault [4].
(ii) Due to the presence of the ac-side capacitors both voltage and current waveforms at the output terminals of a CSC are good sinusoids. The capacitors are the inherent filter for the CSC. The problem of the resonance between the capacitances and inductances on the ac-side can be overcome by careful design of the capacitor based filter circuit and introduction of sufficient damping using proper control methods [5]. Furthermore, all the switching problems faced in the early stages of CSC development can be overcome by employing tri-level switching scheme which has become a standard technique in the control of CSC [6].
(iii) Integrated Gate Commutated Thyristor (IGCT) having high ratings, high reverse voltage blocking capability, low snubber requirements, lower gate-drive power requirements than GTO, and also has higher switching speed than GTO, is the optimum combination of the characteristics demanded in high-power applications [7]. Using the state-of-the-art technology of the semiconductor switches, there will be no need for the series diode in the CSC topology anymore.
(iv) The dc-side losses are expected to be minimized by using superconductive materials in the construction of the dc-side reactor [5].

In comparison with the VSC topology, the application of CSC topology in D-STATCOM is expected to achieve many advantages. The direct output of a CSC is a controllable ac current, whereas that of a VSC is a controllable ac voltage. When operated under SPWM technique [8], the magnitudes of the harmonic components in both converters are directly proportional to the magnitudes of the fundamental components of their direct output quantities. Under the normal operating conditions, the current injected by D-STATCOM is a small percentage of the line current. Hence, when CSC topology is used, the current harmonics are also small. However, when VSC topology is used, for a small injected current, the output voltage of VSC is large and very close to the system voltage. This results in large voltage harmonics, leading to current harmonics that are larger than those generated by CSC, and thus more costly to filter. The other aspect of comparison is the dc-side energy storage requirement. When the D-STATCOM is realized by a CSC, the dc-side current is just larger than the peak value of the required injected current which is a small percentage of the line current. However, when a VSC is used to inject reactive power to the system, the dc-side voltage must be larger than the peak value of the system line-to-line voltage so that the reactive power can be exchanged between the D-STATCOM and the ac distribution system. Hence, the dc energy storage requirement of the CSC topology is expected to be lower than that of the VSC topology when it is used to implement a D-STATCOM system for mitigation of voltage sag.

Although, D-STATCOM can be used for the improvement of quality and reliability of power supplied to consumers in many ways, the aim of this paper is restricted to investigate the performance of a CSC based D-STATCOM for mitigating voltage sag phenomenon which is considered to be one of the well known unwanted power quality problem resulting from sudden change in load connected to a power distribution system as a first step. The simulation results of the proposed model are also presented to validate the model for its suitability in mitigating the voltage sag and provide improved power quality to the end-users.

2 Power quality problems

The term power quality is concerned with deviations of the voltage from its ideal waveform (voltage quality) and deviations of the current from its ideal waveform (current quality). Such deviation is known as “power quality phenomenon” or “power quality disturbance” [9]. Some examples of the power quality problem include- impulsive and oscillatory transients, short duration voltage variations (sag or dip, swell, interruption), long duration voltage variation (undervoltage, overvoltage, sustained oscillation), voltage imbalance, waveform distortion (harmonics, notching, dc offset), voltage flicker, etc. These problems are generally caused by the nature, faults on transmission or distribution system and also by the power consumers. The power transmission lines are exposed to the forces of nature and its loadability limit is usually determined by either stability considerations or by thermal limits. Although the power quality problem is a distribution side problem, transmission lines frequently have an impact on the quality of power supplied. It is however to be noted that while most of the problems associated with transmission systems arise due to the forces of nature or due to the interconnection of power systems, individual customers are responsible for a more substantial fraction of the power quality problems in the distribution side [4]. The flexible ac transmission system (FACTS) and the custom power devices are the two major power electronics based initiatives to counter the power quality problems. Although FACTS and custom power initiations share the same technological base they have different technical and economic objectives. The FACTS controllers are aimed at the transmission level whereas custom power controllers are aimed at the distribution level particularly at the point of connection of the electricity distribution on company with clients having sensitive loads and independent generators. Custom power focuses primarily on the reliability and power quality. However, voltage regulation, voltage balancing and harmonic cancellation may also get benefited from this technology [3].

2.1 Voltage sag and interruption

Although electric power consumers are very much concerned about the issues of power quality, still there is no consensus amongst the various agencies in defining the term power quality. However, it has become a widely used term and it is the best term available at the moment. The term power quality has gained some official status in IEEE through the name of SSC 22 (Standards Coordinating Committee). But the international standards setting organization in electrical engineering, the IEC does not use this term in any of its standard documents instead it uses the term electromagnetic compatibility which is not the same as power quality. However, these two terms has a strong overlap relationship. Power quality is the combination of voltage quality and current quality. It is concerned with the deviations of voltage and/or current from the ideal state. It should be noted that power quality has nothing to do with the deviations of the product of voltage and current (i.e. power) from any ideal shape [9].

The voltage sag is a power quality problem phenomenon which falls under the category of short duration voltage variation. Any variation in the supply voltage (rms) for duration not exceeding 1 min is called a short duration voltage variation. Usually such variations are caused by system faults, energization of heavy loads that require large inrush currents and intermittent loose connection in the power wiring. Voltage sag is a fundamental frequency decrease in the supply voltage for a short duration. The duration of voltage sag varies between five cycles to a minute [4]. The interest in voltage sag is mainly due to the problems caused by several types of equipments viz. adjustable speed drives (ASD), process control equipment, and computers which are highly sensitive. Some of the loads may trip when the rms voltage drops below 90% for longer than 1 or 2 cycles. If this is the process control equipment of a paper mill, one can imagine that the damage due to voltage sags can be enormous. Of course, voltage sag is not as damaging to industry as a (long or short) interruption. But as there are far more voltage sags than interruptions, the total damage due to voltage sags is still larger. Short interruptions and most long interruptions are originated from the local distribution network. However, voltage sags at equipment terminals can also be due to short circuit faults 100 s of kilometers away in the transmission system. Hence, voltage sag is much more of a "global" problem than an interruption. Reducing the number of interruptions typically requires improvements on one feeder and reducing the number of voltage sags requires improvements on several feeders and often even at transmission lines far away [9].

The voltage interruption according to IEEE standard 1159 or just "interruption" according to IEEE standard 1250 is a condition in which the voltage at the supply terminals is close to zero. Close to zero is by the IEC defined as lower than 1% of the declared voltage and by the IEEE as lower than 10%. The voltage interruptions are generally caused by faults which subsequently trigger protection measures. Some other causes include power system protection operation when there is no fault present, broken conductors not triggering protective measures and operator interventions. The voltage interruption can be subdivided based on their durations. The IEC uses the term long interruptions for interruptions longer than 3 min and the term short interruptions for interruptions lasting up to 3 min. However, in IEEE the terms momentary, temporary and sustained interruptions are used [9]. The problem of voltage sag at distribution network can be mitigated by using VSC based custom power devices such as D-STATCOM or dynamic voltage restorer (DVR). In this paper, a CSC based D-STATCOM is proposed for mitigating the voltage sag.

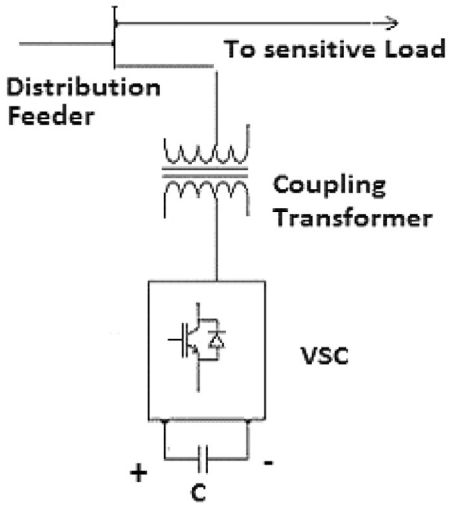

Figure 1. Schematic diagram of a VSC based D-STATCOM.

2.2 D-STATCOM configuration

The D-STATCOM is a shunt connected custom power device. If the FACTS device static synchronous compensator (STATCOM) is used in the low voltage distribution system, it is identified as D-STATCOM. However, there is a substantial difference in the operating characteristics of a STATCOM and a D-STATCOM. The STATCOM is required to inject a set of three balanced quasi-sinusoidal voltages which are phase displaced by 120° but the D-STATCOM must be able to inject an unbalanced and harmonically distorted current to eliminate the unbalance or distortions in the load current or the supply voltage. Hence, its control is significantly different from that of the STATCOM. A D-STATCOM is usually configured by using a voltage source inverter circuit interfaced with a coupling transformer and energy storage element viz. capacitor in case of VSC based D-STATCOM as shown in Figure 1. The D-STATCOM used in custom power applications uses PWM switching control as opposed to the fundamental frequency switching strategies which is preferably used in FACTS applications. PWM switching is practically used in custom power applications as it is at relatively low power level [3, 4, 10].

3 CSC based D-STATCOM

The CSC based D-STATCOM can be realized by modifying the basic configuration of the VSC based one. It also consists of a current source inverter circuit which is interfaced

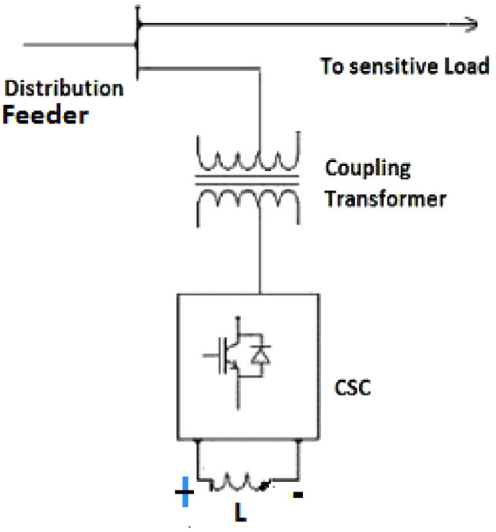

Figure 2. Schematic diagram of a CSC based D-STATCOM.

with a coupling transformer and a dc link reactor/inductor as shown in Figure 2.

On the ac side of the CSC based D-STATCOM capacitors are connected in shunt acting as low pass filter which ensures to provide good sinusoidal output voltage and current waveforms.

3.1 Design considerations of CSC for D-STATCOM

The working principle and control of CSC for use in D-STATCOM is similar to those of the CSC employed in ac motor drives but its design strategy is different to certain extent as listed below:

(a) The CSC circuit will be subjected to voltage regulation problem on the ac side when the reactive power is varied from full inductive to full capacitive, This will affect the voltage rating of the switching devices as well as the design of the input low pass filter (LPF) circuit.
(b) Since the dc link circuit consists only inductor and its internal resistance, the electrical time constant will be high and thus affects the design process of this circuit.
(c) The design objectives of the CSC for use in D-STATCOM is not only to filter harmonics but also to achieve optimal sizing of the CSC so as to meet the control range requirements of the D-STATCOM in both the capacitive and inductive load operating ranges [11]. The selection of switching device and modulation scheme depends on the application voltage and power rating [12]. For applications at transmission level voltage such as FACTS devices, GTO switches are used. At distribution level applications such as D-STATCOM, IGBT switches and PWM scheme can be chosen if VSC topology is used. The converter topology for the proposed model being CSC, switches having sufficient reverse voltage blocking capability should be selected. Unless a switch of sufficient reverse voltage withstanding capability such as Gate-Turn-Off (GTO) thyristor is used, a diode has to be placed in series with each of the switches in CSC. This almost doubles the conduction losses compared with the case of VSC. Hence, GTO switches are used in the proposed model. The schematic circuit diagram of the model consists six number of fully controllable GTO switches represented by S_1, S_2, S_3, S_4, S_5, and S_6 as depicted at Figure 3. These switches are configured in bridge fashion and fed from a dc link reactor acting as a energy storage element. The output of the CSC is filtered by a three-phase LPF comprising of three capacitors connected in shunt manner. The dc link reactor approximates the dc link current I_{dc} to a level current waveform in the steady state. The nearly level dc-link current is converted to bidirectional current pulses alternating at supply frequency in the ac lines of CSC by switching power semiconductor switches in accordance with a pre-specified pattern [13, 14].

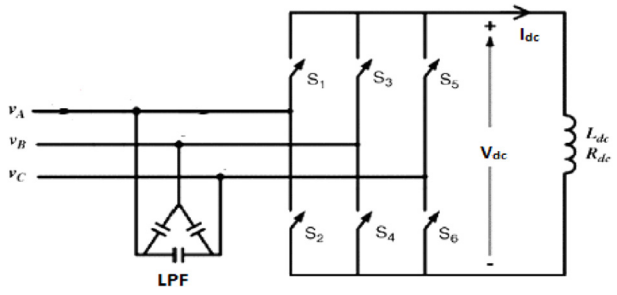

Figure 3. Schematic circuit diagram of CSC.

3.2 Design of dc link reactor and input LPF

In the CSC circuit the energy storage element is an inductor with its internal resistance. The amount of reactive power to be generated by the CSC can be computed from the relation:

$$Q = \sqrt{(3/2)}VMI_{dc}\cos\theta \quad (1)$$

where V = rms value of the fundamental component of converter input line-to-line voltage, M = modulation index, I_{dc} = mean dc-link current and θ = phase shift [11]. Equation (1) indicates that Q is independent of the dc-link inductance L_{dc}. The value of L_{dc} affects the response time of D-STATCOM against the variations of reactive power demand of the load. The time constant of the dc-link circuit τ_{dc} is L_{dc}/R_{dc}. Hence, the value of L_{dc} should be selected as small as possible for allowing rapid rise or decay of mean dc-link current against the rapid changes in Q if the phase-shift angle control at fixed modulation index is used for controlling the reactive power.

The capacitor input low pass filter (LPF) is connected at the output of the CSC for feeding sinusoidal ac voltage after separating higher order harmonic components to the coupling transformer. The leakage impedance of the coupling

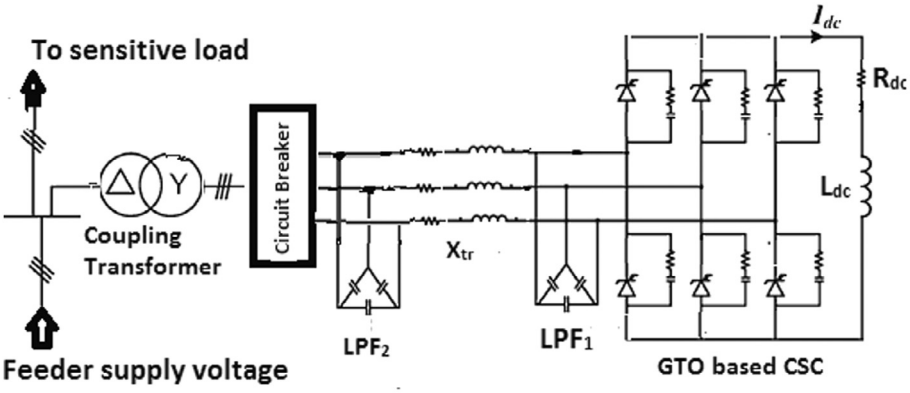

Figure 4. Simplified structure of the proposed D-STATCOM implementation.

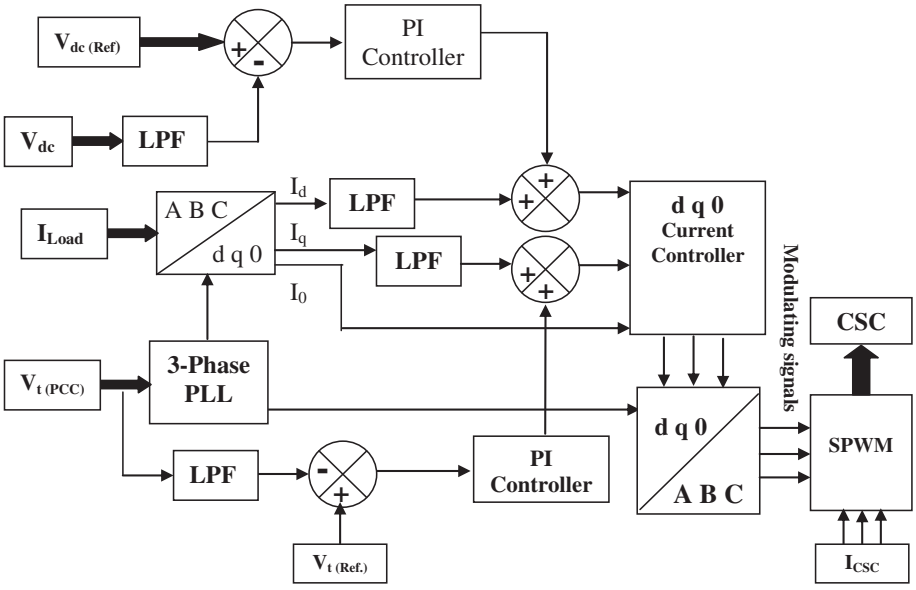

Figure 5. Control scheme block diagram for the proposed D-STATCOM.

transformer also behaves as a part of the LPF. External series reactors (i.e. X_{tr} in Figure 4) have been used on the low voltage side of the coupling transformer for adjusting the corner frequency of the input filter to an optimum value for the fixed shunt connected capacitor in implementing the proposed D-STATCOM. The corner frequency should be chosen as small as possible for better performance of the filter circuit. The detailed design strategies of the LPF are available at [14].

3.3 Control scheme

For generating proper gating signals of the GTO switches used in the CSC, SPWM control scheme is chosen for the proposed model. The SPWM switching strategy has constant switching frequency capability. This constant switching frequency reduces stress levels on the converter switches [16]. The control scheme will able to maintain constant voltage magnitude at the point where a sensitive load is connected under system disturbances. The control system only measures the rms voltage at the point of common coupling (PCC) and no reactive power measurements are carried out. The CSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. As the distribution network operates at a relatively low-power application, such method offers a more flexible option than the fundamental frequency switching method used in FACTS applications. The block diagram of the control scheme designed for the proposed model is shown in Figure 5. The commonly used control schemes for the generation of reference source currents in most of the VSC based D-STATCOM include instantaneous reactive power theory (IRPT), synchronous reference frame theory (SRFT), unity power factor (UPF) based, instantaneous symmetrical components based, etc. [16]. The control scheme chosen for the proposed D-STATCOM model is based on SRFT. The load currents, I_{Load} (i_a, i_b, & i_c), the PCC voltage $V_{t(PCC)}$ (v_a, v_b, & v_c), and the reactor dc voltage (v_{dc}) of D-STATCOM are sensed and used as feedback signals. The load currents from the *a-b-c* frame are first converted to the α-β-0 frame

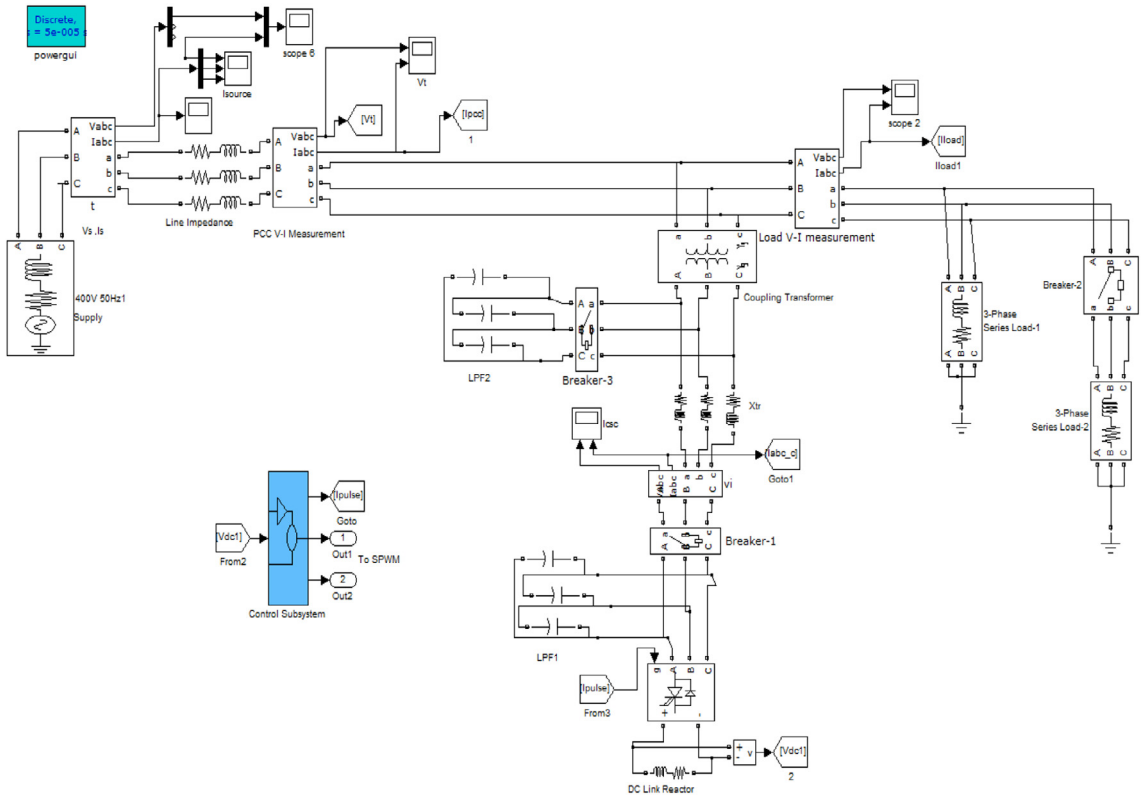

Figure 6. Test set up of the proposed CSC based D-STATCOM.

Table 1. Various parameter settings of the model under simulation.

Sl. no.	Name of the component	Parameter values
1.	Feeder system voltage	$V_{t(PCC)}$ = 400 V (rms), 50 Hz
2.	Feeder system reference voltage	$V_{t(Ref.)}$ = 328 V(rms), 50 Hz
3.	Feeder impedance	R_f = 0.01 Ω, L_f = 2 mH
4.	DC reference voltage	$V_{dc(Ref.)}$ = 1 kV
5.	DC link reactor of CSC	L_{dc} = 8000 mH, R_{dc} = 0.01 Ω
6.	AC side LPF_1 shunt filter capacitor of CSC	C = 2.85 mF
7.	AC side LPF_2 shunt filter capacitor of CSC	C = 8.5 mF
8.	AC side external reactor, X_{tr}	R = 0.01 Ω, L = 1 mH
9.	Inductive $Load_1$	R = 0.06 Ω, L = 8000 mH
10.	Inductive $Load_2$	R = 0.06 Ω, L = 98 000 mH
11.	DC link voltage PI controller	$K_{P(dc)}$ = 0.25, $K_{i(dc)}$ = 0.14
12.	AC system voltage (at PCC) PI controller	$K_{P(q)}$ = 0.4, $K_{i(q)}$ = 0.5
13.	SPWM switching frequency	f_s = 20 kHz

and then to d-q-0 frame by using the Park's transformation relation as:

$$i_d = \frac{2}{3}[i_a \sin\theta + i_b \sin(\theta - 2\pi/3) + i_c \sin(\theta + 2\pi/3)] \quad (2)$$

$$i_q = \frac{2}{3}[i_a \cos\theta + i_b \cos(\theta - 2\pi/3) + i_c \cos(\theta + 2\pi/3)] \quad (3)$$

$$i_0 = \frac{1}{3}[i_a + i_b + i_c] \quad (4)$$

where cos θ and sin θ are obtained by using the three-phase phase locked loop (PLL). The PLL receives signal from PCC terminal voltage $V_{t(PCC)}$ for generation of fundamental unit vectors for conversion of sensed currents to the d-q-0 reference frame. The SRF controller extracts dc quantities by a LPF and removes the harmonics from the reference signal. The distribution feeder terminal voltage $V_{t(PCC)}$ is regulated by a PI controller after comparing $V_{t(PCC)}$ with a reference terminal voltage $V_{t(Ref.)}$ which produces a i_q signal and adds with i_q generated at equation (3) and acts as reference component for the current controller. The error signal output after comparing with the dc link reactor voltage V_{dc} with a

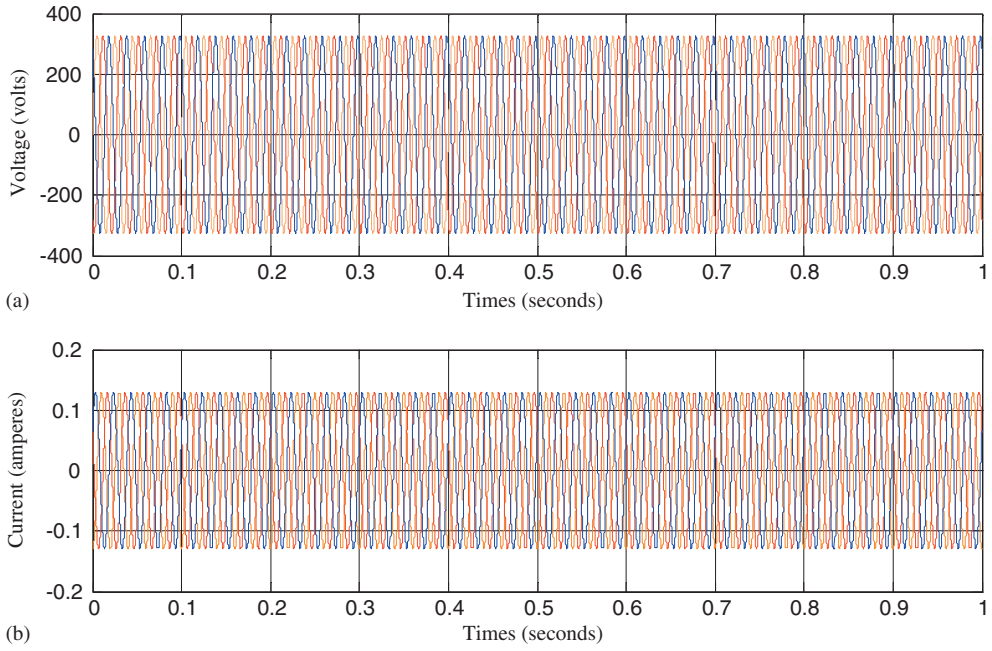

Figure 7. Load voltage and current waveforms under steady state condition.

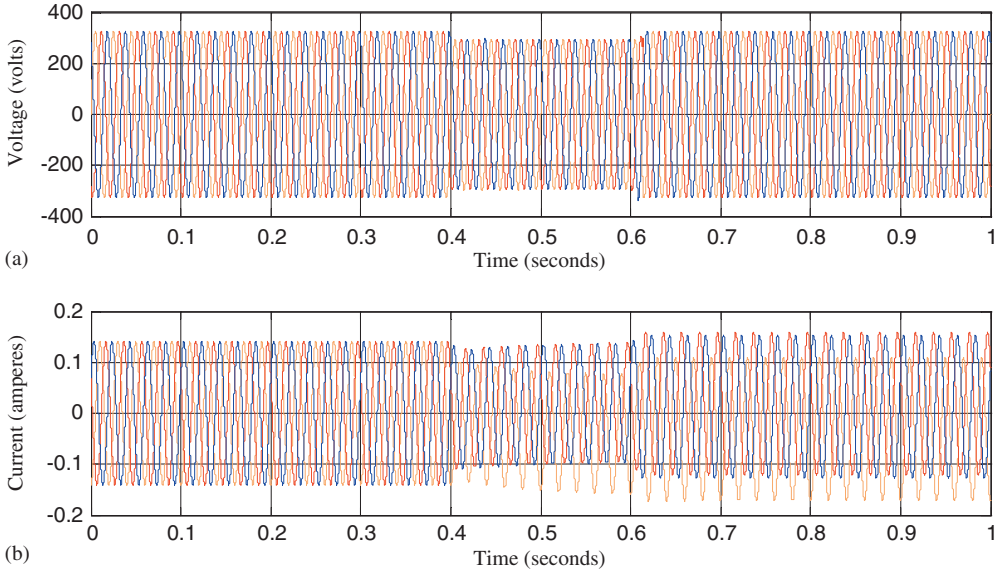

Figure 8. Load voltage and current waveforms under abnormal load condition without D-STATCOM.

$V_{dc(Ref.)}$ is processed by another PI controller to regulate the dc link voltage and produces i_d current component. This current is added with the i_d available at equation (2). The reference source current must be in phase with the voltage at the PCC but with no zero-sequence component and it can be obtained by using reverse Park's transformation process as discussed in reference [15]. The sensed current and the reference source current are compared and a proportional controller is used for amplifying current error in each phase in the current controller. The SPWM generates gate drive pulses for the six number of GTO switches used in the CSC based D-STATCOM.

4 Model simulation and results

The Matlab/Simulink model of the proposed CSC based D-STATCOM shown in Figure 6 has been simulated under steady state (with normal load) and dynamic (sudden change in load) conditions. The various parameter settings of the model are listed at Table 1.

The output voltage and current waveforms under different conditions are presented below:

(a) *Simulation results under steady state* (*with normal load*): The D-STATCOM and the second heavily inductive

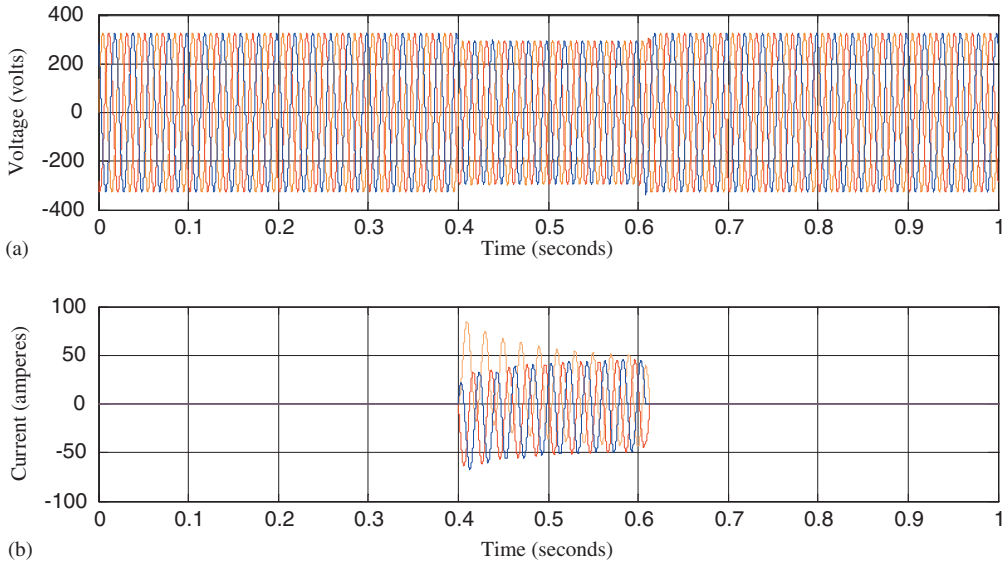

Figure 9. Voltage and current waveforms under heavily inductive load condition at PCC without D-STACOM.

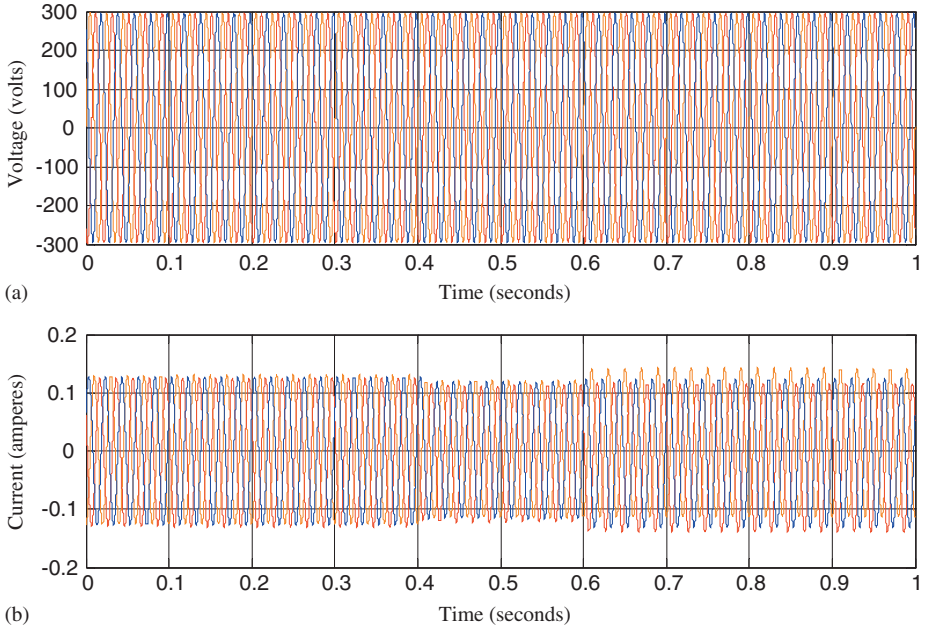

Figure 10. Voltage and current waveforms under sudden change in load condition with D-STATCOM.

three-phase load are disconnected from the power distribution system by opening the three-phase circuit breaker 1 and 2 respectively and the model is simulated. Figure 7 shows the voltage and current waveforms under steady state condition. Figure 7a depicts the voltage waveform across the load and Figure 7b shows the current waveform in the load. From this simulation result, it is observed that there is no voltage sag taking place across the load. The magnitude of voltage and current are found to be 360 V and 0.14 A respectively.

(b) *Simulation results under load perturbation* (*with sudden change in load*): For observing the profile of the voltage and the current waveforms under sudden change in load condition, the D-STATCOM is disconnected by opening the circuit breaker 1 and the second heavily inductive three-phase load is connected by closing the three-phase circuit breaker 2. The circuit breaker 2 closing transition time is set from 0.4 to 0.6 s. Figures 8a and 8b show the load voltage and current waveforms respectively. Under this condition, a voltage sag with magnitude of 340 V which is 20 V less than the non-sag voltage magnitude for a duration from 0.4 s to 0.6 s appears across the load as shown in Figure 8a. Figure 9 shows the voltage and current waveforms at the point of common coupling (PCC) without operating the D-STATCOM.

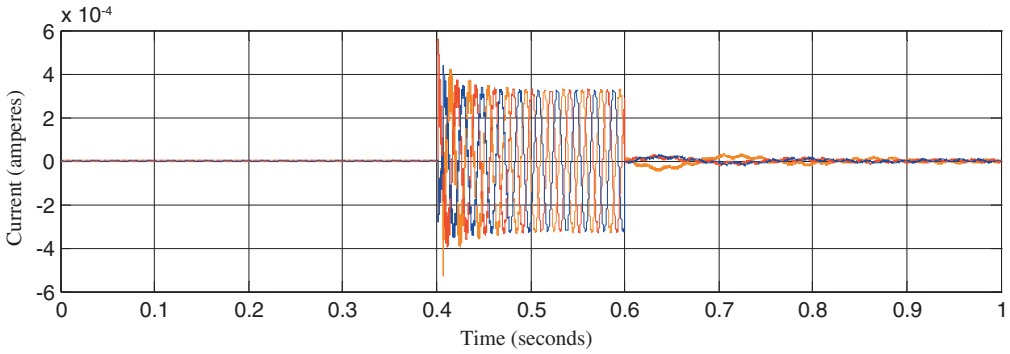

Figure 11. Injected current waveform from the D-STATCOM during voltage sag mitigation process.

(c) *Simulation results under load perturbation with the D-STATCOM*: In order to mitigate the voltage sag taking place due to the introduction of sudden change in load, the D-STATCOM is brought to operation by closing the circuit breaker 1 with its transition time setting from 0.4 s to 0.6 s and the model is simulated. Figures 10a and 10b depict the load voltage and current waveforms. It is observed that the load voltage sag during the period from 0.4 s to 0.6 s have been effectively mitigated by the proposed D-STATCOM under this condition. The voltage profile of the load can be improved by connecting the LPF_2 though the operation of circuit breaker 3 of the circuit diagram. For reducing the overall cost of the ac side filter, LPF_2 may be eliminated or kept as optional. Figure 11 shows the injected current waveform from the D-STATCOM during the process of mitigating the load voltage sag.

5 Conclusions

In this paper, a current source converter based D-STATCOM has been modeled and simulated with the objective of mitigating voltage sag occurring in the event of sudden change in load condition at power distribution system. The use of CSC topology in the custom power applications which has not been the focus of many researchers for a long time due various reasons is explored through this paper. From the simulation results of the proposed model, it is learnt that the voltage sag at the distribution level voltage under load perturbation has been successfully mitigated by introducing a CSC based D-STATCOM system instead of using a VSC based one. This paper will pave the way for encouraging the application of the CSC topology in other types of custom power devices for solving power quality problems. Some examples of the possible power quality problems where CSC topology can replace the VSC include voltage swell, unbalance, harmonics, power factor correction, etc.

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