Fault Tolerant Control: Application of GIMC structure to a PLL Identifier Module

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Abstract – In this paper, we present a study dealing with stabilizing and robust controllers synthesis, precisely the Fault Tolerant Control (FTC). The case where these controllers are calculated by GIMC (Generalized Internal Model Control) structure will be developed and applied to a Phase-locked Loop (PLL) Identifier Module. In each case, we will focus on the control and the system output evolutions in the defects event. We will show the control quality and the advantages offered by GIMC structure in the transitory mode and the permanent one.

Key words: Fault Tolerant Control, stability, residue, GIMC structure, Phase Locked Loop (PLL).

1 Introduction

In order to ensure the systems reliability and human safety, the problem of systems control with presence of defects was largely studied by several researchers. The major part of research was devoted to study the Fault Detection and Diagnosis (FDD) problem and so the determination of the system's operating condition (Normal or defected), Iserman [1].

Under the assumption of a block of diagnosis providing information related to the detection and the localization of the defect, it is possible either to compensate the defect effect (accommodation) or to reconfigurate the control laws in order to bring the system in the possible nearest state to its normal one(called commonly reconfiguration or reorganization). These procedures to be implemented at the time of the defect occurrence were developed by several strategies defined under the expression of the Fault Tolerant Control Systems FTCS), Iserman [1] and Eterno [2].

This paper will be organized as follows. Section 2 studies the Fault Tolerant Control problem. Section 3 presents the GIMC structure. Section 4 gives a basic theory of Phase-Locked Loop Identifier Module. Finally, in section 5 a numerical example is illustrated showing the results.

2 Fault Tolerant Control (FTC)

The purpose of the FTC is to put up itself automatically with the effect of the defects while being able to maintain the stability and at best the nominal performances of the system. The consequence is to avoid the immediate system's arrest and to allow its function in a degradation mode. The FTC is generally classified into two distinct approaches: a passive approach (Passive Fault Tolerant Control, PFTC) and an active approach (Active Fault Tolerant Control, AFTC).

2.1 Passive methods

PFTC methods use the techniques of the robust control to ensure that the closed loop system remains insensitive to certain defects with constant regulators and without using online defects information on the system, Eterno [2]. This approach doesn't require a diagram of fault detection nor a control law reconfiguration but its tolerance capacity remains limited to some defects.

2.1 Active methods

The first active methods of accommodation were developed and applied in the aeronautics field of beginning in year 80. Contrary to the passive methods, the active methods react to the appearance of one or several defects by the reconfiguration of the control system. Their main aim is as to compensate the fault effect of the defects on the system so that the stability and the performances are maintained while exploiting the robustness of the control which must be improved with each detection of a defect.

These methods, Thabet [3], are based on one of the following principles: the linear quadratic control, the pseudo reverse method, the adaptive control, the predictive control, techniques by multi-models, Fuzzy logic/Neuronal networks. In this work, we will present GIMC structure as an AFTC method.

3 Generalized Internal Model Control structure

The parameterization of Youla offers an adequate architecture for the design of an AFTC law, Youla [4]. This parameterization allows description the whole of all the correctors stabilizing a system and satisfying a given performance level. The idea is to use H∞ standard synthesis to elaborate a nominal corrector and the parameterization of Youla to parameterize it, in order to make it robust and to respect a class of predetermined defects. The latter are then considered as model uncertainties (multiplicative defects) or exogenic disturbances (additive defects).

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To formalize this idea, we consider $G_0(s) \in \Re H_\infty$, the matrix of transfer obtained starting from the state representation (A, B, C, D) of the nominal system:

$$G_0 = C(sI - A)^{-1}B + D$$

Supposing that K_0 is a corrector stabilizing G_0, and then it exists left and right factorizations coprimes, $U, V, \tilde{U}, \tilde{V}, \tilde{M}, \tilde{N}, M$ and N such as:

$$\begin{aligned} K_0(s) &= U(s)V(s)^{-1} = \tilde{V}(s)^{-1}\tilde{U}(s) \\ G_0(s) &= \tilde{M}(s)^{-1}\tilde{N}(s) = N(s)M(s)^{-1} \end{aligned} \quad (1)$$

Any regulator K stabilizing G_0 can then be deduced from $\tilde{U}, \tilde{V}, \tilde{M}, \tilde{N}$ and a transfer matrix Q called Youla parameter. The structure of K is illustrated on the following figure (Fig.1). We note K_0 is the regulator corresponding to the particular choice $Q = 0$ and called central corrector.
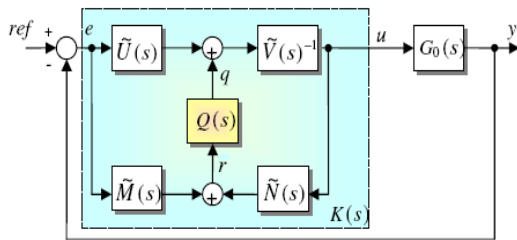

Fig. 1. Youla Parameterization

The idea consists in rewriting the structure of Fig.1 the way illustrated by Fig.2 and to synthesize the Youla parameter Q such as the control law is tolerant to the defects, Cieslak [5]. This particular structure is called GIMC structure (Generalized Internal Model Control structure). We can notice on Figure 1 that if we choose $Q = 0$, we find the central corrector. Considering the vector of residues as being defined in the following general form, Zhou [6]:

$$r(s) = \tilde{N}(s)u(s) - \tilde{M}(s)y(s) \quad (2)$$

where: $\tilde{M}$ and $\tilde{N}$ define a decomposition coprime on the left model of the system under G_0 normal functioning.
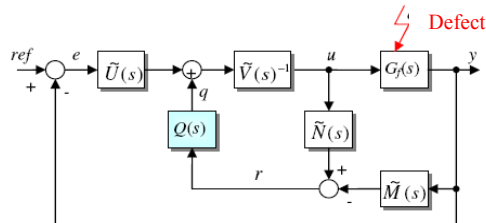

Fig.2. GIMC Structure

r can be used as a defect indicating signal. The control law illustrated on Fig.2 is then written as a function of the residue vector r:

$$u(t) = \tilde{V}(s)^{-1}(\tilde{U}(s)e(t) + r(t)) \quad (3)$$

This illustrates well the philosophy of AFTC since the control depends now on the residue vector. So that Q can be synthesize either starting from the objectives of diagnosis or starting from the objectives of control, or by managing a compromise between the performances specifications in control and diagnosis. In this paper, the idea of using the Youla parameterization of which was taken again by Delgado [7] and [8] to accommodate the failures actuators and sensors is interesting.

$$G_f(s) = G_0(s) + W_1(s)\Delta_f(s)W_2(s), \Delta_f \in H_\infty \quad (4)$$

where G_0 indicate the nominal system given by the state representation (A, B, C, D), G_f present failing system. Δ_f is an unstructured uncertainty block modeling the defects such as $\|\Delta_f\|_\infty \le 1$. W_1 and W_2 are selected ponderation in an adequate way. Thus $G_f(s) = (I + \Delta_f(s))G_0(s)$ with $W_1(s) = G_0(s)$ and $W_2(s) = I$ representing the sensors defects, and $G_f(s) = G_0(s)(I + \Delta_f(s))$ with $W_1(s) = I$ and $W_2(s) = G_0(s)$ representing the actuators defects. The objective is to synthesize the Youla parameter Q minimizing the influence of the defects effect on the system with the H_∞ direction. In a formal way, this problem is written as:

$$Q = \arg \min \|T_{zw}\|_\infty \quad (5)$$

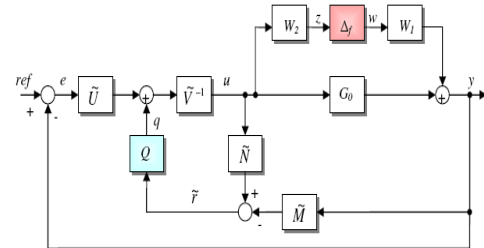where T_{zw} is the transfer function in closed loop of $w \rightarrow z$ (see Fig.3)

Fig.3. GIMC structure with multiplicative defects.

The solution to this problem is then given by the following theorem:

Theorem 1 (Delgado [7])

Supposing that $W_1(s), W_2(s) \in \Re H_\infty, G_0(s) \in \Re H_\infty$ and $K_0(s) = \tilde{V}(s)^{-1}\tilde{U}(s)$ is a corrector stabilizing G_0 while ensuring a certain closed loop performance. Then, the relation:

$$Q(s) = -\tilde{U}(s)\tilde{M}(s)^{-1} \quad (6)$$

is the optimal solution to the optimization problem (5) where $\tilde{M}$ and $\tilde{N}$ are the left decomposition coprime of G_0. Indeed, for this choice of Q, the criterion (5) is null.

However, it is not always desirable to have the compensation signal q active all the time. In fact, authors show that the solution (6) doesn't guarantee neither the robustness against model errors, nor the robustness against exogenic disturbances. To resolve this problem, the authors propose to adopt a FTC structure where the compensation signal q is added to the nominal control signal since the fault detection and location. The activation of FTC strategy is carried out

using commutation logic (see Fig.4). Whereas FTC corrector is in open loop for a no failing situation. It is important to mention that with the Figure 4 configuration, the closed loop system is not linear any more due to the introduction of commutation logic into the loop. This logic gives a hybrid character to the closed loop system and returns its analysis of complex stability. No real solution to this problem is presented by the research. The latter simply propose to operate commutation only once and to maintain it until the operation cycle in progress is finished.
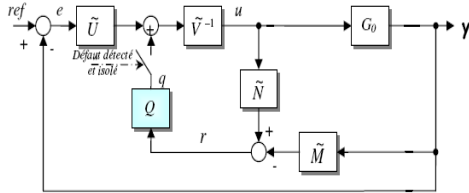
Fig.4. GIMC structure with commutation logic.

4 Phase-Locked Loop Identifier Module- Basic Theory:

Phase-locked loops have been used in a number of applications ranged from speed control loops to the detection of FM signals for radio receivers. The analysis of phase-locked loop systems used in the above applications has been covered in detail by a number of authors, Crowe and Johnson [9]. In the application of a phase-locked loop to system identification, Crowe and Johnson [9] and [10], the loop is used to extract the phase information from the process under test and provide the appropriate excitation for the system. The phase-locked loop system which was first devised was based on a number of ideas implemented as an analogue circuit as shown in Fig.5.
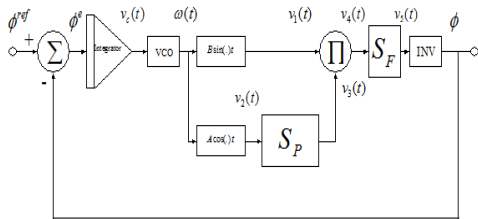

Fig.5. Phase-locked loop identifier module - Analogue prototype

The identifier module of Fig.5 was conceived as a feedback circuit around a voltage-controlled oscillator (VCO). The reference input to the loop was the desired process phase angle, so to drive the loop towards the critical frequency, the phase reference is $\phi^{ref} = -\pi$. Thus at the comparator, the phase error signal input to the integrator is given by $\phi^{e}(t) = \phi^{ref}(t) - \phi(t)$. The integrator in the loop is designed to ensure that the constant phase reference signal is attained in steady state conditions. The integrator equation is straightforwardly $v_c(t) = \int_0^t \varphi^e(\tau)d\tau$. A voltage-controlled oscillator produces the sinusoidal excitation sig-

nals of appropriate frequency. This frequency is proportional to the integral of phase reference error, $\omega(t) = K_{VCO}v_c(t)$, where the gain of the voltage controlled oscillator is denoted, K_{VCO}. The voltage-controlled oscillator generates two sinusoidal signals, $v_1(t) = B \sin \omega t$ and $v_2(t) = A \cos \omega t$. The signal $v_2(t)$ is used to excite the process and after transients have decayed, yields the steady state output signal,

$$v_3^{SS}(t) = S_p(v_2(t)) = A \left| G_p(j\omega) \right| \cos(\omega t + \varphi(\omega)) \quad (7)$$

Across the multiplier, the steady state output is,

$$v_4^{SS}(t) = v_1(t) v_3^{SS}(t)$$
$$= \frac{AB}{2} \left| G_p(j\omega) \right| \left[\sin(2\omega t + \varphi(\omega)) - \sin \varphi(\omega) \right] \quad (8)$$

This signal is used in the nonlinear block to extract and identify the phase achieved by the current frequency value. This current value of the phase is then fed to the comparator to complete the loop. The amplitude A of the process excitation signal is user selected to minimize disruption to the process outputs. The equation for $v_4^{SS}(t)$ shows that a convenient choice for amplitude B is to use $B = 2/A$. In this way, the dependence of the signal $v_4^{SS}(t)$ on signal amplitudes A and B through the multiplier $AB/2$ is removed. The concepts in this analogue prototype were used to construct a phase-locked loop identifier module that retained the feature of continuous-time process excitation and used digital processing in the data extraction components of the outer loop.

All the sinusoidal signals in the module below (Fig.6) are transformed and adapted in square signals (SSC) and the comparator of phase used is a pump charges(PPC), Acco [11], and this module be used in the application.
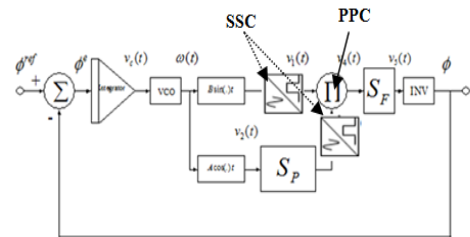

Fig.6. Phase-locked loop identifier module using adapted signals

5 Application

Considering the system with following transfer function

$$H(s) = \frac{1}{0.0032 * s + 1}$$

(Frequency for -45°=50Hz). Parameters of the loop are: the VCO gain is $K_{VCO} = 0.25$Hz/V, the filter used is 1 st order

(low-pass) such as its cut-off frequency is $2\pi rad / \sec$; the current Ic of pump Charge is 1A. For a reference phase equal to -45°, we will present the evolution of the various sizes of the loop in the case without defects:

According to Fig.7 we note dephasing between the signal exciting the system to be identified and that of output (dephasing of -45°) in permanent mode.
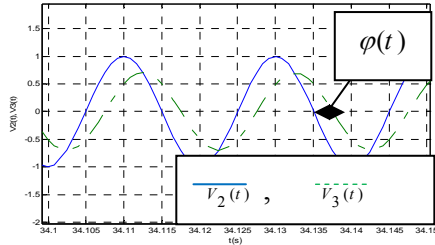

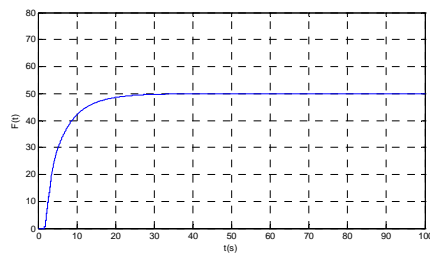Fig.7. Evolution of $V_2(t)$ and $V_3(t)$ in permanent mode
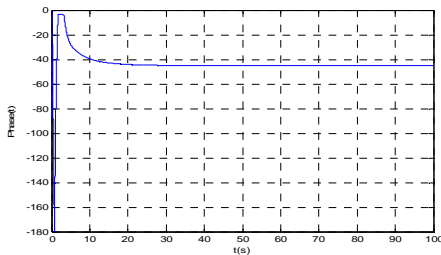

Fig.8. Frequency evolution $F(t)$
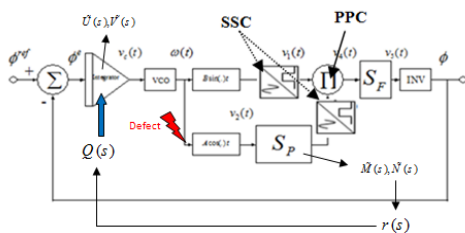

Fig.9.a. Phase evolution $\varphi(t)$

Fig.9.b. Application of GIMC structure on the module

Fig.8 and Fig.9.a show well the control quality of the frequency and the phase for the same reference phase.

We inject then a defect on the actuator of the loop (on the system input variation from + 3: very strong excitation on the static gain of the actuator which is almost equal to 3 times its face value) between the moments 20s → 25s (transitory mode) and we observe the variation of the loop controlled variables with and without application of the GIMC structure.

1 - For the decomposition [5] we choose $L=1,(A-LC)$ and $F=1,(A-BF)$ for the transfer function and the regulator nominal also, such as: $\tilde{M}(s)=\dfrac{s+312.5}{s+313.5}$ and

$\tilde{N}(s)=\dfrac{625}{2s+627}$, $K_0(s)=\dfrac{1}{s}$ the regulator nominal of the loop, from where: $\tilde{U}(s)=\dfrac{1}{s+1}$ and $\tilde{V}^{-1}(s)=\dfrac{s+1}{s}$ thus:

$Q(s)=-\dfrac{s+313.5}{s+312.5}$, for the commutation logic we have chosen a binary test on value 0 of the residue ($r\neq 0$).

2 - The application diagram of GIMC structure on the module is showed as in Fig. 9(b).

In a first place we observe the residue $r(t)$ variation indicating the occurrence of a defect:
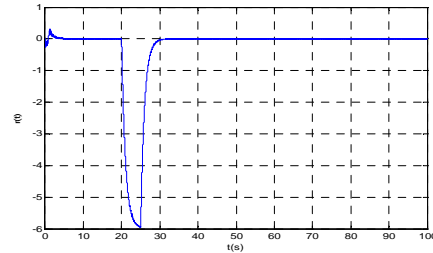

Fig.10. Residue variation $r(t)$

In a second place, we notice according to these figures above, during the presence of the defect (application of the defect in transitory mode), that for the case where we applied GIMC structure and according to Fig.11: the frequency evolution is better than that at faulty case since it is not of strong value of frequency (maximum at fault $F_{GIMC}(t)=51,4Hz$ however, for the preceding case is almost $F_d(t)=68Hz$); The control loop variation (Fig.12): $Vc_{GIMC}(t)$ is about 20% of that in nominal case while $Vc_d(t)$ is about 47%, thus the elimination of the actuator's over-excitation risk.
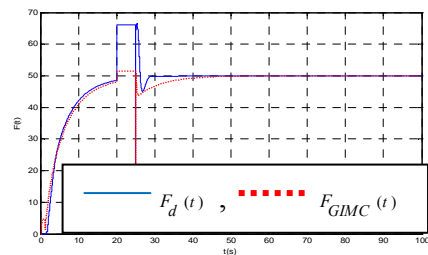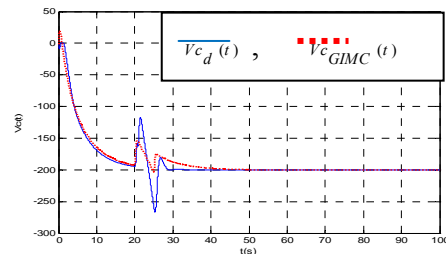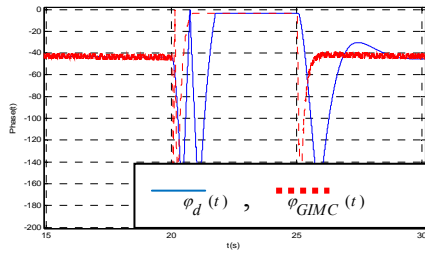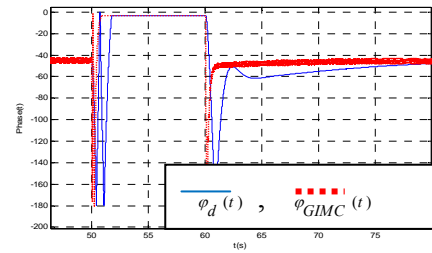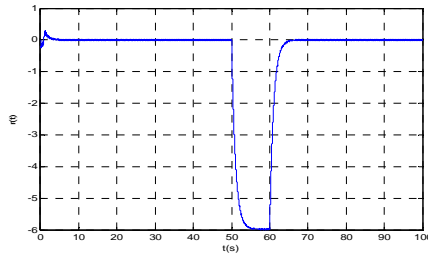

Fig.11. Frequency variation : $F_d(t)$ and $F_{GIMC}(t)$

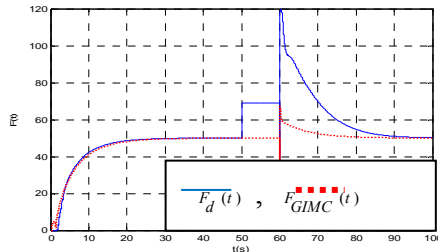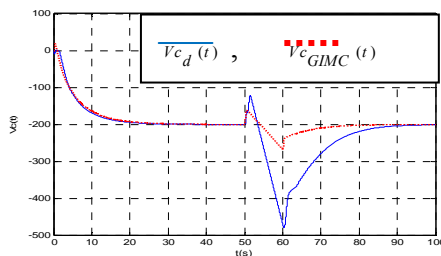Fig.12. Loop control variation $Vc_d(t)$ and $Vc_{GIMC}(t)$

According to Figure 13, the module output variation (the phase) is better while applying GIMC structure. It offers a stabilization time better:

$Td_{stabilization}=29s$ and $T_{GIMC\,stabilization}=26s$.

Now, we inject the same defect but at the moments 50s →60s (permanent mode) and we observe the system Outputs/Inputs variations.

Fig.13. Phase variation: $\varphi_d(t)$ and $\varphi_{GIMC}(t)$

Fig.14. Residue variation $r(t)$

We notice according to Figures 15-17, during the presence of the defect (application of the defect in permanent mode), that for the case where we applied GIMC structure, we see almost same qualities and performances offered in the application of the method to the transitory mode with Just small value variations (Fig.15 and 16).

Fig.15. Frequency variation $F_d(t)$ and $F_{GIMC}(t)$

Fig.16. Loop control variation $Vc_d(t)$ and $Vc_{GIMC}(t)$

The only exception is the frequency variation and according to Fig.17 we see that:

$$T_{d_{stabilization}} > T_{GIMC_{stabilization}}.$$

Thus the solution offered by GIMC structure makes it possible to avoid strong deviation of frequency and maintains it near the rated frequency even in faulty case (an increase of 2.8%) as well as a small variation of the Loop control eliminating the risk from unhooking of the loop and a better phase control, from where a solution allowing to maintain as well as possible the nominal performances of the system in the occurrence of a defect even if this defect is injected into the transitory mode.

Fig.17. Phase variation: $\varphi_d(t)$ and $\varphi_{GIMC}(t)$

6 Conclusion

In this work, we proposed an application a method of AFTC called: GIMC structure on Phase-locked Loop Identifier Module. This application has presented very important results, showing, clearly, the quality of control and performances which are closer to that of nominal case and an acceptable control value at the defects occurrence. The results obtained seem to be encouraging and consequently, this application can be used in the case of the PLL regulators auto-parameter setting, Crowe and Johnson [10].

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