Int. J. Simul. Multidisci. Des. Optim. **2**, 123–133 (2008)

DOI: 10.1051/smdo:2008017

Available online at:
http://www.ijsmdo.org

Reliability of the connections used in IGBT modules, in aeronautical environment

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Received 24 December 2007, accepted 26 March 2008

Abstract – In this paper, two IGBT modules assembling technologies with double side cooling capabilities and high level of integration were proposed for aeronautic applications after a state of the art and failures analysis. These technologies are compared using design of experiment based on non-linear finite element analysis with various materials, with respect to their potential failures under thermal and power loading profiles. The configurations optimizing the lifetime and reliability level were pointed out by loading profile and failure mode. Recommendations were then done in order to choose the optimal configuration of assembly for each application. Finally, these design rules were followed by the study of parts dimensions effects on the design outputs in order to help dimensioning the IGBT modules.

Key words: Power electronic packaging; constitutive laws; failures criteria; FEM; DoE.

1 Introduction

Within the framework of the electric plane programs which policy aims at replacing hydraulic actuators by electric ones for weight reduction and reliability improvement, the aircraft industry is facing a higher demand of electric power, fact which involves an increasing use of IGBT modules in power converters. Although such modules have been well studied and known in railway and the automotive domains, they will be subjected to stresses and operational cycles specific to the aeronautical environment. It was predicted that these modules will be used in harsh environment as in the engine nacelle, near the actuators they supply. Consequently, this requires manufacturers to answer some questions about their lifetime and reliability issues.

Many works studied solders lifetime [1] and evaluated modules reliability by probabilistic approaches [2], but the question of an optimal design for a specific application was usually studied by packaging techniques overviews.

The objective of this work is to propose specific technologies of IGBT modules, materials choice and mechanical dimensioning rules, for aeronautic applications.

To tackle this problem, the followed steps consist in analyzing the failures observed in railway and automotive environments, (wire bonding lift-off, solders crack, substrates delamination...), in order to propose solutions concerning connection techniques and materials more appropriate to aeronautical operational environment. Two sandwich assemblies with ceramic substrates and metallizations, brazed on two base plates for double side cooling capabilities were proposed, with respect to aeronautic criteria.

These technologies were then compared with different materials chosen according their availability and in compliance with regulations about the use of hazardous substances [1].

In aeronautic applications, IGBT modules can be considered as operating under a combination of two loading profiles: a power loading at chips levels when switched at high frequency to ensure good input and output current waveforms, and a thermal loading due to environmental temperature variation.

For both profiles, Design of Experiments method was used basing on non-linear Finite Element Modelling results regarding the chips junction temperatures (thermal impedances), the chips and ceramic substrates brittle fracture (maximal principal stresses) and the critical solders joints fatigue (Inelastic Strain Energy Densities – ISED). A 2^3 factorial design built according to the Yates algorithm helped reducing the number of simulations while getting the maximum information on how materials and their interactions affect the module design outputs. The most significant factors with their effects were pointed out for each yield response, and then recommendations were proposed.

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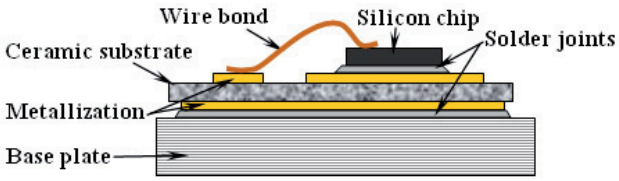

Fig. 1. Structure of a wire bonding IGBT module.

Then, an analysis was performed on module geometrical parameters (bumps sizes and layers thicknesses) to determine how they affect the yield responses. This second analysis brought additional information about the effect of these parameters design rules for each specific application.

2 IGBT modules technologies overview

For high power electronic applications, such as in power transmission, industrial drives, and locomotive traction control systems, many IGBT modules packaging approaches were proposed by industrials and research laboratories. The most common of these technologies are presented hereafter, with their main advantages and drawbacks.

2.1 Wire bonding connection module

This approach is the most used in IGBT module packaging. The chips are brazed on a metallized substrate and base plate, the electrical connections being achieved by wire bonds (Fig. 1). These wires bonds are main cause of failure under power cycling [3] as depicted in Figure 2. Large solder joints cracks (Fig. 3a) are main failures mode under thermal cycling [4]. As shown in Figure 3b, the delamination starts at solder joint corners, causing thermal impedance degradation and then chip excessive heat [5]. The substrates and silicon chips also exhibits high risk of brittle fracture. Other concerns with the use of this technology in aeronautical environment are about the worst electromagnetic compatibility due to high parasitic inductances, the poor thermal management and low integration level. Some other approaches were proposed.

2.2 Pressure pack module

Sandwich assembly with chips pressed between two attachments flanges with molybdenum interleaving part to accommodate the coefficients of thermal expansions (Fig. 5). This technology exhibits a good reliability because of the absence of solder joints, a good thermal management but needs special isolation and cooling systems, leading excessive weight and cost.

2.3 Layer connection technologies

This approach was first proposed in 2001 by General Electric [6], the chips are mounted on metallized substrate with top connections obtained by alternating conducing and dielectric layers (Fig. 6). Other variants of this technology are Planar Power Polymer Packaging (General Electric – 2004) and Embedded Power (CPES – 2004) [7]. Despite of the good electrical and thermal performances with high integration level, these approaches exhibit high parasitic capacitances and require complex and delicate manufacturing processes.

2.4 Bump array contact modules

This technology is based on chips brazed on metallized substrate, the connections being realized by solder bump arrays (Fig. 7). Many variants of this technology were proposed. The most known of this approach are Dimple Array Interconnexion (CPES – 2004) [6], Flip Chip on Flex (CPES, General Electric – 2004) [6] and Power Bump Connection (Eupec, PEARL – 2004). This approach presents a better integration level and thermal management compared to wire bonding technology, but requires complex and delicate manufacturing processes. Questions about lifetime of connection solders during thermal cycling also need to be answered.

2.5 Direct solder contact module

This approach first investigate in 2000 by INPG – LEG, CEA – LETI and Alstom Technology – PERT [8], aims at improving the thermal impedance and reliability by balancing the module structure [9]. The chips are sandwiched by two metallized substrates with connections by direct solder (Fig. 8). Despite of the good electrical and thermal performances with high integration level [8, 10], this technology needs designers to answer questions about dielectric withstand, because of the low distance between metallizations.

3 Choice of IGBT modules configurations

Selection criteria were defined on the basis of thermal and thermomechanical efficiency, (chips connection possibilities, integration level, thermal management, electromagnetic compatibility, weight, volume, materials safe operating areas and toxicities, cost, processing...). Two sandwich technologies with Power Bump (PB) (Fig. 9) and Direct Solder (DS) (Fig. 10) connection technique were retained. Both assemblies allow double side cooling with good integration levels.

3.1 Potential failures modes

From mechanical point of view, two main failures are susceptible to occur in these technologies: solder joints thermomechanical fatigue and brittle materials (ceramics and

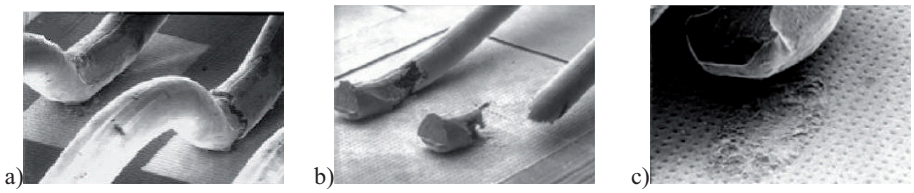

Fig. 2. Rupture (a), corrosion (b), and lift-off (c) of wire bonds [3].

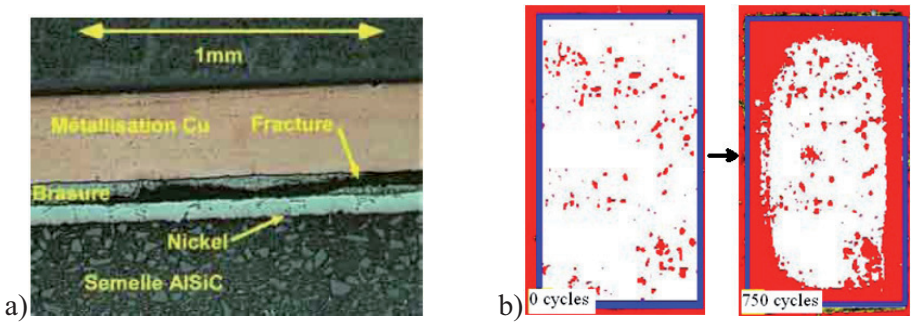

Fig. 3. Base plates solder fatigue fracture (a) [4], and delamination progression (b) [5].

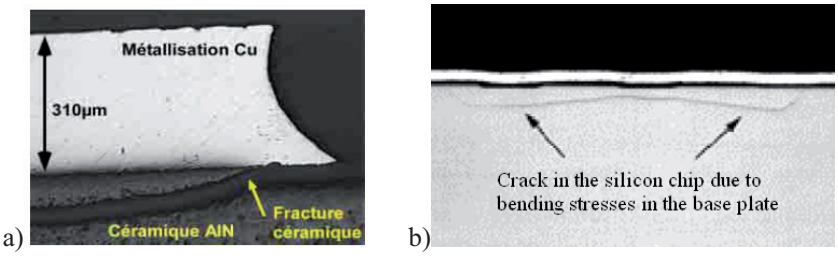

Fig. 4. Fracture of ceramic substrates (a) [4] and silicon chip (b) [3].

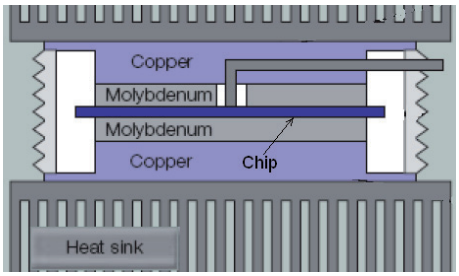

Fig. 5. Pressure Pack assembling stack.

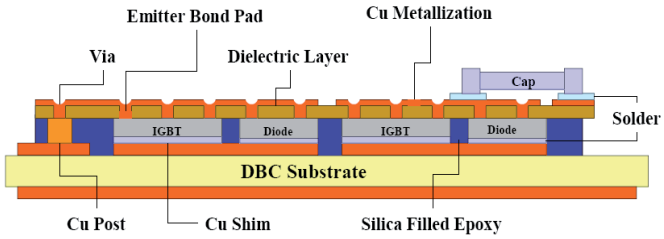

Fig. 6. Power Overlay Technology (General Electric – 2001).

silicon chips) fracture. Beside these failures, the electronic components (IGBT and Diodes) failures by excessive heat due to poor thermal management were also taken into account.

3.2 Materials

The two basic assemblies will be compared with different materials chosen according to their availability, their compliance with aeronautic criteria and with the directives RoHS and WEEE on the use of hazardous substances in electrical and electronics equipments [1, 11].

Aluminium nitride (AlN) and silicon nitride (Si_3N_4) ceramic substrates were retained with copper and aluminium as metallizations. The assembling process of these packaging requires the use of two solders with high and low melting point. According to their good mechanical strength, melting points and wetting properties, the eutectic $Sn_{96.5}Ag_{3.5}$ were retained for all the connections, except the chips bottom (collectors or anodes) solders which are realized with $Pb_{92.5}Sn_5Ag_{2.5}$ solder. Two metal matrix composites (Al-SiC(63%) and Cu-C(40) [12]) are considered as base plates.

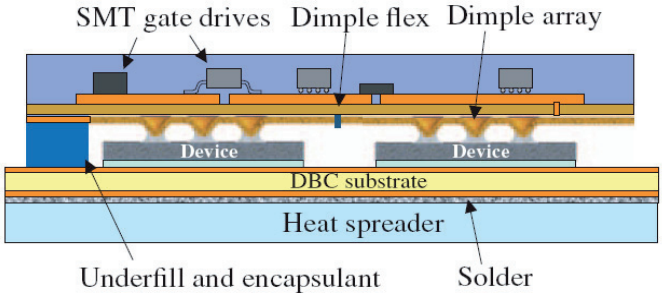

Fig. 7. Dimple array interconnexion (CPES – 2004).

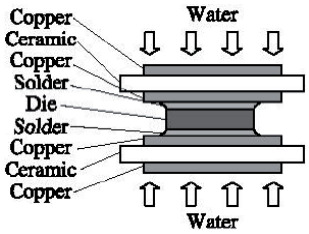

Fig. 8. Direct solder contact module [8].

Table 1. Base plates constitutive laws parameters [4, 12].

	Al-SiC(63%)	Cu-C(40)
λ (W/(K m))	175	300// 160⊥
C (J/(kg °C))	741	420
ρ (kg/m^3)	4000	6100
CTE (10^{-6}/K)	7.9	8.5
E (GPa)	192	75
ν	0.24	0.3

4 Materials thermal and mechanical behaviour

Thermal and mechanical properties were gathered from literature researches, for all the materials regarding their operating conditions, melting point, yield stress, Ultimate Tensile Strength (UTS), Coefficients of Thermal Expansion (CTE), etc.

4.1 Ceramics and metallizations

The base plates thicknesses lead stresses to remain in their elastic domains. Linear elastic law was used to model their mechanical behaviour. The corresponding material law parameters are presented in Table 1.

As suggested by Dupont in [4], elastoplastic law with linear kinematic hardening was used to model metallization mechanical behaviour. Table 2 shows the corresponding material parameters.

4.2 Silicon chips and ceramic substrates

Regarding the observed failures at their level, and their traditional operating conditions, these materials will be modelled with elastic linear law, with brittle fracture.

Table 2. Metallization constitutive laws parameters [4].

	Aluminium	Copper
λ (W/(K m))	220	398
C (J/(kg °C))	880	380
ρ (kg/m^3)	2700	8850
CTE (10^{-6}/K)	24	17.3
E (GPa)	70.6	128
ν	0.34	0.36
Yield Stress (MPa)	17.8	98.7
Tangent modulus (MPa)	350	1000

Table 3. Chips and ceramics constitutive laws parameters [4].

	Silicon chip	AlN ceramic	Si_3N_4 ceramic
λ (W/(K·m))	146	190	60
C (J/(kg·°C))	750	750	800
ρ (kg/m^3)	2330	3300	3290
CTE (10^{-6}/K)	2.5	4.5	3.3
E (GPa)	130	344	310
ν	0.22	0.25	0.27
UTS (MPa)	200	400	800

Many models based on weakest link theory were proposed to describe the ceramics rupture [13]. These approaches need the material parameters to be identified, but a more simple way is to consider the Rankine's (maximal principal stress) criterion which is widely sufficient within a comparison purpose. The corresponding material parameters are given in Table 3.

4.3 Solders joints

The solders, operating at temperatures above the third of their melting points, were described using Anand's unified viscoplastic model [14].

This law was not available in ABAQUS^{TM} Software, it was integrated according to the steps suggested by [15], and implemented via the user interface UMAT. A FORTRAN subroutine, calculating the stress increment and material Jacobian matrix, knowing the strain field, was written. Simulations and verifications with various solders revealed that there are good agreements between the user subroutine and bibliography results presented in [16, 17]. Table 4 lists hereafter the two solders constitutive laws parameters.

Concerning the solders fatigue, inelastic dissipation is believed to better capture the accumulated damage. Many authors proposed cyclic Inelastic Strain Energy Density (ISED) based models for solders joints lifetime prediction [1, 18]. These models show that the number of loading cycles before solder failure is a monotonic decreasing function of the ISED dissipated per cycle. The analysis of the various assembling configurations is for this reason done hereafter according to the ISED dissipated in solder joints per loading cycle.

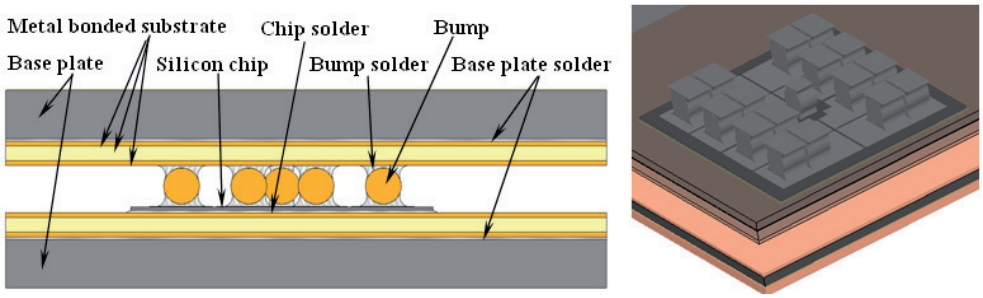

Fig. 9. Power Bump (PB) assembly (Infineon 1200 V – 150 A chip).

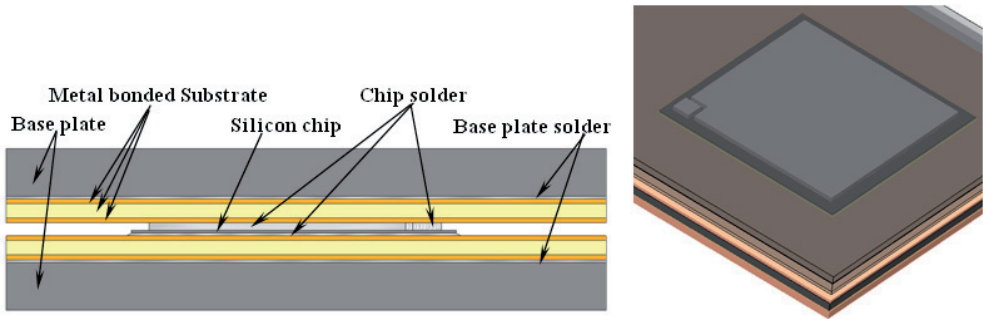

Fig. 10. Direct Solder (DS) assembly (ABB 1200 V – 150 A chip).

Table 4. Solders constitutive laws parameters [16,17].

	$Pb_{29.5}Sn_5Ag_{2.5}$	$Sn_{96.5}Ag_{3.5}$
λ (W/(K m))	35	33
C (J/(kg °C))	129	200
ρ (kg/m^3)	11300	7360
CTE (10^{-6}/K)	29	30.2
E (MPa)	$24028-28{\cdot}T(^\circ\mathrm{C})$	$47200-191{\cdot}T(^\circ\mathrm{C})$
ν	0.44	0.4
Anand's Parameters		
s_0 (MPa)	33.07	7.72
Q/R (K)	11024	14100
A (s^{-1})	105000	1630000
ξ	7	1.61
m	0.241	0.13
h_0 (MPa)	1432	58700
$\hat{s}$ (MPa)	41.63	11.99
n	0.002	0.017
a	1.3	2.09

5 Numerical design of experiment

With respect to the potential failure modes and loading profiles, nine design responses were defined and considered for this analysis: thermal impedances for chips junction temperatures, maximal principal stresses for chips and ceramic substrates brittle fracture, and the inelastic strain energy densities for critical solders joints fatigue, for both loadings profiles. Table 5 lists the responses considered, with their given labels.

The nine plans was built following the Yates algorithm [19], 3 factors listed in Table 6, with 2 levels each other, were considered with their first order interactions. The responses calculations were performed with the non-linear finite element models presented below.

5.1 Finite element modelling

Two parameterised finite element models (Fig. 11) generated using python scripts under ABAQUS^{TM} were used. The geometries of the elementary modules are based on standard thicknesses used in automotive and railway domains: base plates (3 mm), ceramic substrates (635 μm) metallizations (300 μm), base plate solder joints (100 μm) bumps cylinders (ϕ 1.4 mm $\times$ 1.5 mm) and direct connection solder joints (200 μm).

Three-dimensional solid linear brick and tetrahedron elements were used for meshing the geometry, the interfaces being supposed perfect.

As suggested by Guédon-Gracia et al. in [20], the assembling process and storage were simulated for the various configurations in order to compute residual stresses across the whole assemblies before cycling. The two loading profiles considered are presented below.

5.1.1 Power cycling

To model the power cycling, 250 W heat dissipation was generated in the whole volume of the IGBT chip within relative short cycles as shown in Figure 12. An overall heat transfer coefficient corresponding to water cooling, at 70 °C reference temperature was applied on the two external sides of the base plates as boundary conditions.

Table 5. DoE responses definition.

Responses	
$Y1$	Thermal impedance
$Y2$	Base plate solder cyclic ISED under thermal cycling
$Y3$	Chip solder cyclic ISED under thermal cycling
$Y4$	Substrate stress ratio (max. stress/UTS) under thermal cycling
$Y5$	Chip stress ratio (max. stress/UTS) under thermal cycling
$Y6$	Base plate solder cyclic ISED under power cycling
$Y7$	Chip solder cyclic ISED under power cycling
$Y8$	Substrate stress ratio (max. stress/UTS) under power cycling
$Y9$	Chip stress ratio (max. stress/UTS) under power cycling

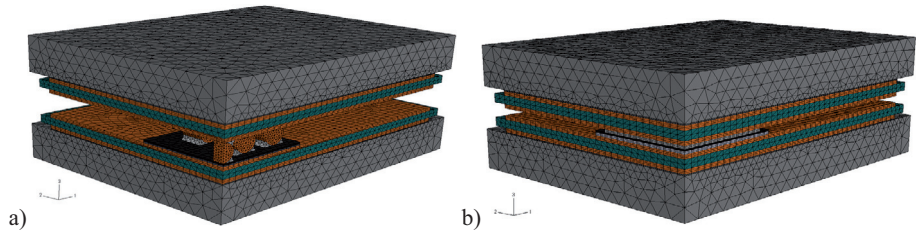

Fig. 11. Elementary power bump (a) and direct solder (b) modules finite elements models.

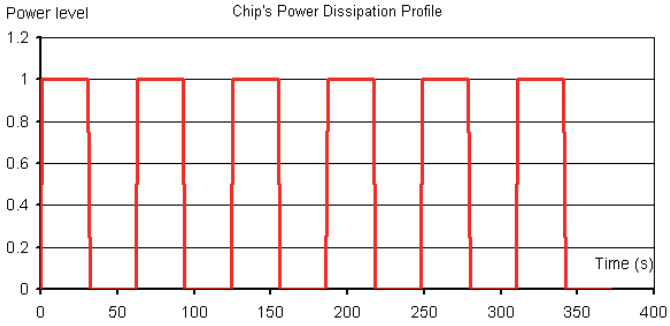

Fig. 12. Power cycling profile.

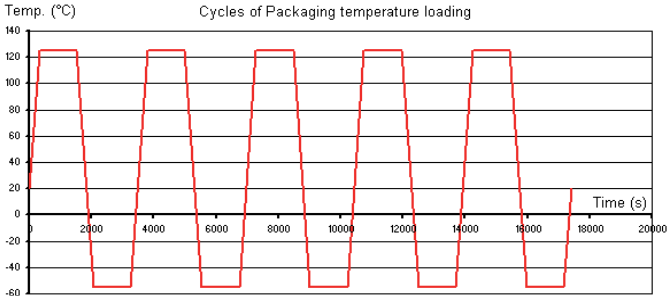

Fig. 13. Thermal cycling profile.

Table 6. DoE factors and levels.

Factors		Levels	
		-1	1
A	Connection	PB	DS
B	Metallization	Copper	Aluminium
C	Ceramic Substrate	Si_3N_4	AlN

5.1.2 Thermal cycling

The International Standard of Atmosphere (ISA) gives the aircraft external temperature profile during a flight cycle. To represent these loadings, an accelerated thermal profile defined according to the Military Standard Handbook 883F was considered.

As depicted in Figure 13, the profile starts at 25 °C, the ramp rate was 20 °C/min and the dwell time at −55 °C and 125 °C was 20 min.

5.2 Simulation results

The heat flux balance across assemblies and the thermal impedances were evaluated from the power cycling simulations (Fig. 14). The thermal impedances ($Y1$) were calculated from the chip maximal temperatures, measured after the steady state is reached. For all the configurations, the design responses $Y4$, $Y5$, $Y8$ and $Y9$ were computed by the ratio of maximal principal stresses in the ceramic substrates (Fig. 15) and chips (Figs. 16 and 17), over their mechanical strengths.

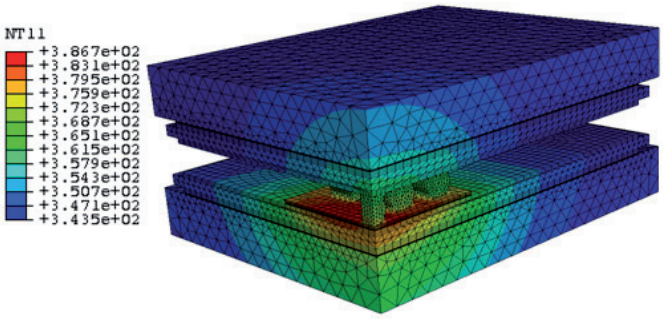

Fig. 14. Temperature distribution in solder bump assembly (K).

The maximal principal stress in the ceramic substrate is localized at the periphery of the bonded metallization.

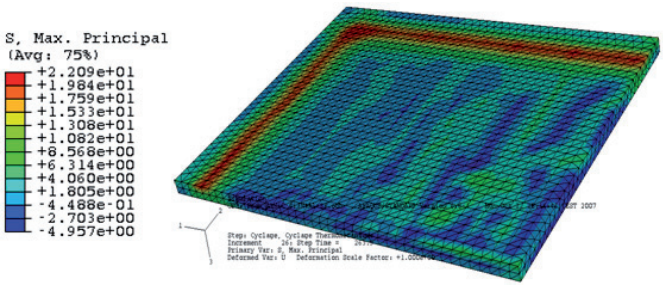

Fig. 15. Maximal principal stress distribution in ceramic substrate (MPa).

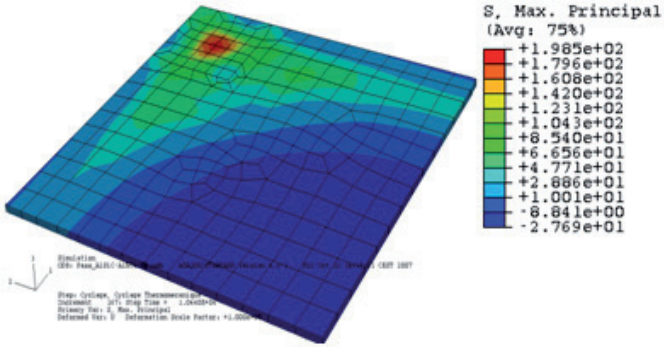

Fig. 16. Maximal principal stress distribution in silicon chip with DS connection (MPa).

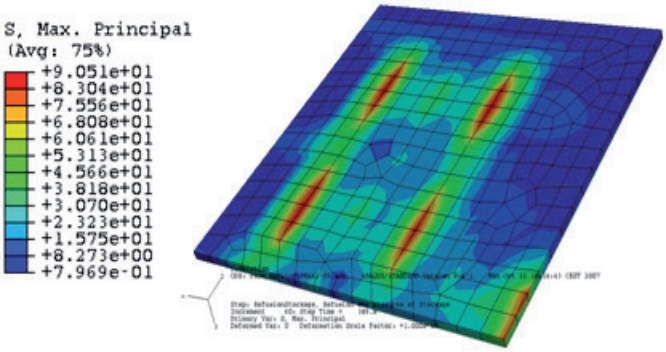

Fig. 17. Maximal principal stress distribution in silicon chip with PB connection (MPa).

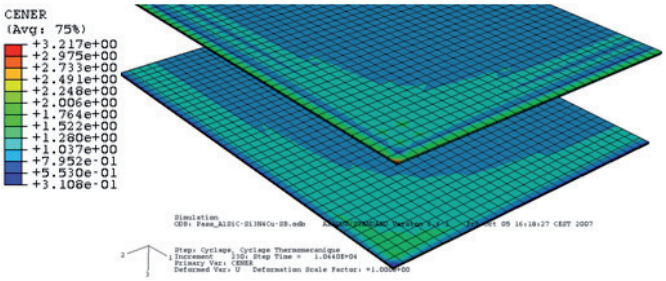

Fig. 18. ISED distribution in base plate solder after thermal cycling (mJ/mm^3).

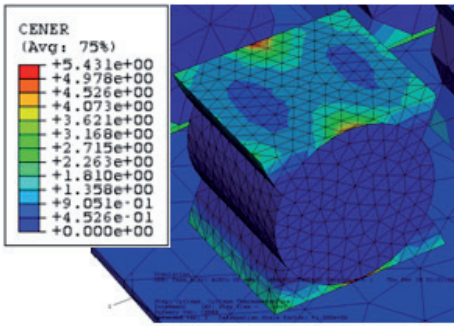

Fig. 19. ISED distribution in bumps solder after thermal cycling (mJ/mm^3).

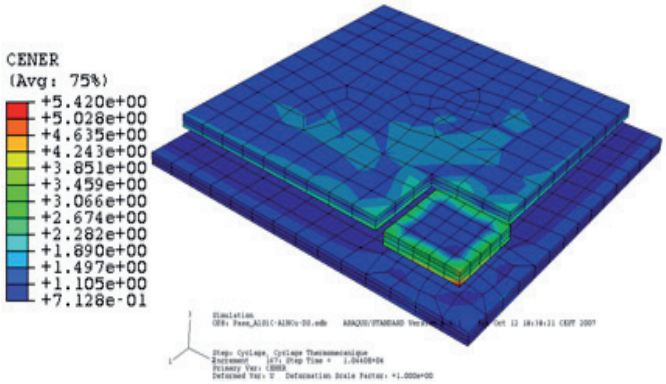

Fig. 20. ISED distribution in direct connection solder after thermal cycling (mJ/mm^3).

In the chips, the maximal principal stress were localized around bump contacts for solder bump connection (Fig. 16) and just under the gate for direct solder connection (Fig. 17).

In order to evaluate $Y2$, $Y3$, $Y6$ and $Y7$, inelastic strain energy densities were computed over the solder joints (Figs. 18–20). Many works [5] showed that the crack in large area solders propagates from solder joint corner (Fig. 3b). The ISED distribution in base plate solder (Fig. 18) is consistent with this result, and then, for more accuracy in this analysis, $Y2$ and $Y6$ were evaluated in the corner elements instead of the whole solder joint.

Regarding connection solders, the ISED were found to be maximal in the bump solder in solder bump assemblies (Fig. 19) and in the gate solder for direct solder assemblies (Fig. 20). Due to the relative small size of these solders, $Y3$ and $Y7$ were evaluated in their whole volume.

As observed in Figure 21, the inelastic strain energy density accumulation per cycle, quickly reaches a saturated value within three loading cycles. This observation allows reducing the computation time, by calculating $Y2$, $Y3$, $Y6$ and $Y7$ within the third cycle, while having good accuracy on the results.

5.3 DoE results and analysis

Basing on simulation results, the effects of the factors were evaluated for the nine responses. A student test with a risk of 5% helped identifying the most significant factors for the nine models. All the 9 responses models built

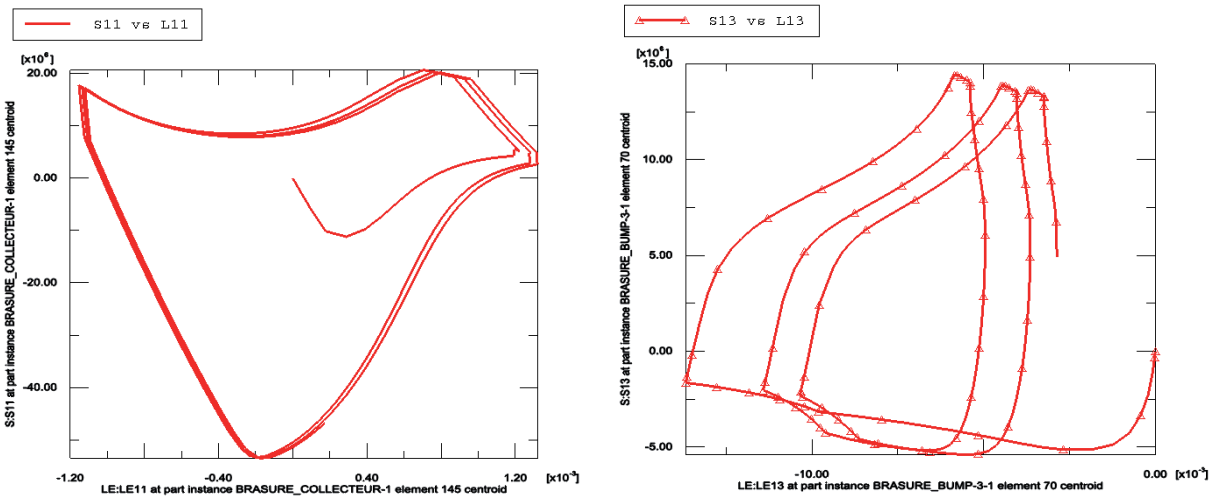

Fig. 21. Normal and shear stress versus strain, during thermal cycling without residual stresses computation.

with the identified factors passed successfully a Fischer-Snedecor test with a 5% risk. Table 7 sums these results, with the significant effects highlighted in bold.

The assembling configurations minimising the design responses, and therefore maximising the modules lifetimes and reliabilities were then identified with respect to the loading profiles.

5.3.1 Thermal impedance and fluxes balance

It appears that the three factors are significant, without their interactions. Direct solder connection with AlN substrate and copper metallization should be preferred, but considering the intrinsic contribution of the metallization within the thermal impedance model (4.6%), aluminium could be an excellent alternative. The fluxes should be more balanced across the assemblies in order to minimize thermal stress concentrations. Regarding this characteristic, direct solders assemblies are superior with 47% of thermal flux balance through bottom and 53% through top cooling faces, compared to solder bump ones which lead to a partition of 26–74%. Other simulation with the two base plates showed that Cu-C is superiors than Al-SiC with about 6.3% of thermal impedance improvement.

5.3.2 Base plates solder fatigue

The only significant factors are the ceramics and metallizations. The use of AlN substrate with aluminium metallization reduces significantly the inelastic strain energy density for both loading profiles. Regarding base plates, Cu-C are superiors than Al-SiC in power cycling, due to their better thermal performances, but less interesting in thermal cycling because of higher coefficient of thermal expansion.

5.3.3 Chip connections solder fatigue

Only aluminium metallizations are recommended for thermal cycling. Considering power cycling loading, direct solder connection, AlN substrate with copper metallization should be recommended.

5.3.4 Ceramic fracture

The stress ratio in the ceramic only depends on the metallization and the ceramic substrate for both loading profiles. Aluminium and Si_3N_4 ceramic minimises ceramic cracking failures risk.

5.3.5 Chip fracture

During thermal cycling, the recommendations are direct solder connection, AlN substrate with aluminium metallization. None of the factors considered have not significant effects on chips stresses during power cycling.

5.4 Discussion

Some contradiction appears in the above analysis when trying to take into account the recommendations for all the responses and loading profiles together. To solve these contradictions, the materials choices could be done with respect to the most critical design outputs and the most preponderant profile, knowing that IGBT modules really operate under a combination of thermal and power loadings. The significant effects presented in Table 7 could then help doing the appropriate design.

The direct solder connection assembly with aluminium bonded AlN appears as the most consensual configuration.

A good solution could be the use of AlN substrate with copper bonded at the chip side and aluminium bonded at base plate side, with suitable thicknesses in order to avoid substrates fracture by bimetallic effect.

Table 7. DoE effects and significance test results.

Responses	I	A	B	C	AB	AC	BC
$Y1$	0.152	−0.031	0.007	−0.013	−0.002	0.003	−0.001
$Y2$	471749	1927	−14631	−16313	−2083	−342	2487
$Y3$	319290	27350	−51018	−13670	4212	−278	−2644
$Y4$	0.138	0.005	−0.046	0.040	0.008	0.001	−0.018
$Y5$	0.621	−0.054	−0.006	−0.046	−0.047	−0.006	0.005
$Y6$	31656	−713	−29262	−7259	821	861	6989
$Y7$	15983	−7660	2198	−4235	−855	1775	−418
$Y8$	0.109	0.001	−0.029	0.032	−0.004	−0.001	−0.008
$Y9$	0.399	−0.035	−0.037	−0.040	−0.078	−0.034	−0.012

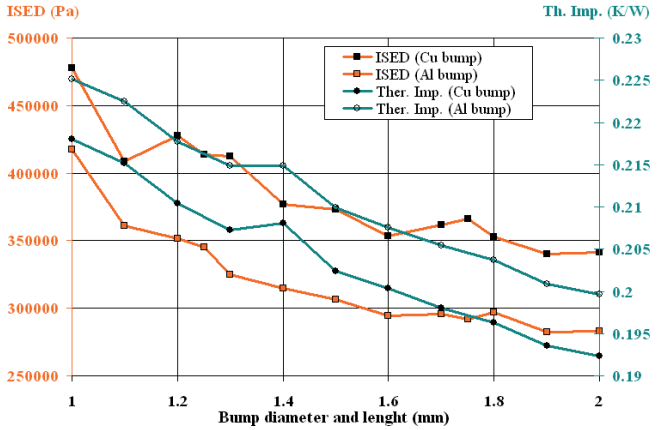

Fig. 22. Evolution of bump solders ISED and module thermal impedance with bump size and material.

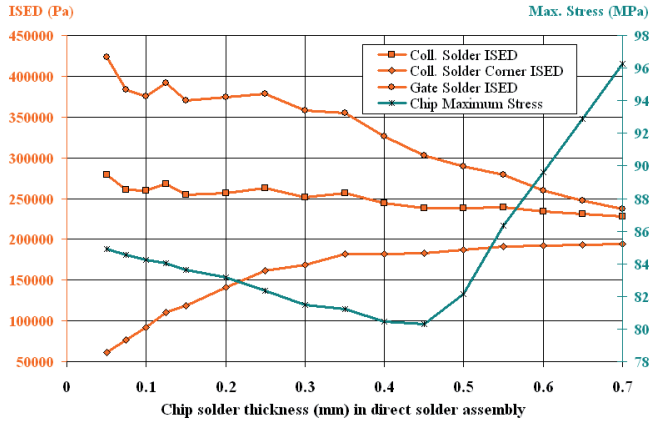

Fig. 23. Evolution of direct connection solders ISED and chip maximal principal stress with chip solder joint thickness.

6 Influence of geometric parameters on module lifetime

The objective of this study is to investigate how the thicknesses of base plate solder, metallizations, ceramic substrates, direct connection solder and bumps dimensions affect the module lifetime. For this purpose, different parameterized models with four IGBT chips, AlN substrates and Al-SiC base plates were generated under ABAQUS^{TM} using python scripts. The results are presented here after.

6.1 Bump nature and sizes

The design parameters chosen for sizing the bumps were the module thermal impedance and the bump solders fatigue. Two materials (cooper and aluminium) were considered with sizes (diameter and length) varying from 1 to 2 mm. Figure 22 presents the evolution of two design parameters for the two kinds of bump. It appears that the module thermal impedance and bumps solder cyclic ISED decrease with the bump size. Moreover, the use of aluminium bump instead of copper reduces bump solders cyclic ISED of about 18% while increasing the thermal impedance of about 3.6%.

6.2 Direct connection solder thickness

The design parameters chosen for sizing the solder thickness were the module thermal impedance, the chip maximal stress and the solder joints fatigue. The simulations were done with thicknesses varying from 50 to 700 μm. As presented in Figure 23, the inelastic strain energy density seems to be constant in the whole chip solder joint, while increasing in the corners. The gate solder joint which is the most critical, decreases with the solder thickness. The chip maximal principal stress presents a minimum for a solder joint thickness around 0.45 mm, but the module thermal impedance increases with a rate of about 0.132 K/(W mm).

6.3 Base plate solder thickness

The design parameters chosen for sizing the base plate solder thickness were the module thermal impedance and the base plate solders fatigue. The simulations were done with thicknesses varying from 20 to 300 μm. Figure 24 presents the evolution of the two design parameters considered. The thermal impedance increases linearly with a rate of 0.122 K/(W mm), while the cyclic ISED seems to be constant when calculated in the whole solder joint, but quickly decreases at the corners until 0.1 mm before decreasing linearly with a rate of about 187 000 Pa/mm.

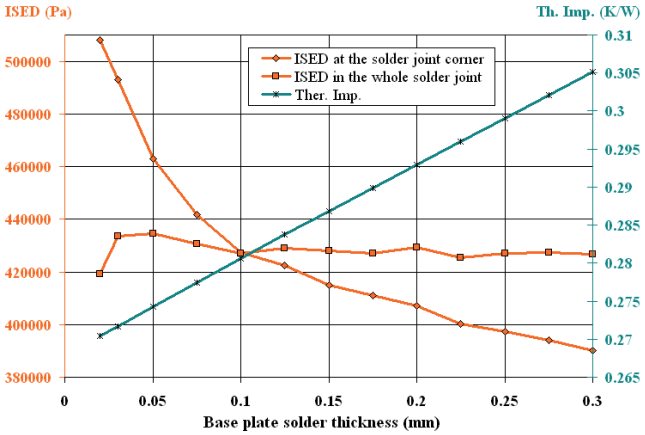

Fig. 24. Evolution of base plate solder ISED and module thermal impedance with base plate solder thickness.

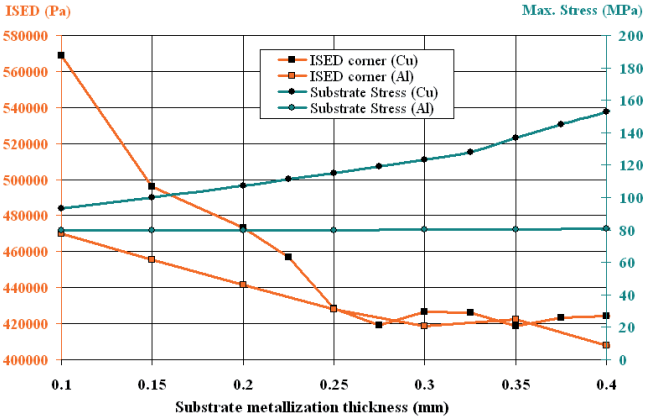

Fig. 25. Evolution of base plate solder corner ISED and substrate maximal principal stress with metallization nature and thickness.

6.4 Metallization nature and thickness

The design parameters chosen for sizing the metallization thickness were the module thermal impedance, the substrate maximal stress and the base plate solders fatigue. Two materials (cooper and aluminium) were considered, the simulations being done with thicknesses varying from 100 to 500 μm. Figure 25 presents the evolution of cyclic ISED at the corner of base plate solder joint. The maximal principal stress in the substrate seems to be constant with aluminium metallization, but increases linearly with copper metallization with a rate of about 150 MPa/mm. Regarding the module thermal impedance, it evolves linearly, with a rate of 0.004 K/(W mm) for aluminium and -0.037 K/(W mm) for copper metallization.

6.5 Substrate thickness

The design parameters chosen for sizing the substrate thickness were the module thermal impedance, the substrate maximal stress and the base plate solders fatigue. The simulations were done with thicknesses varying from 200 to 1400 μm. The maximal principal stress in the ceramic decreases with the substrate thickness (Fig. 26),

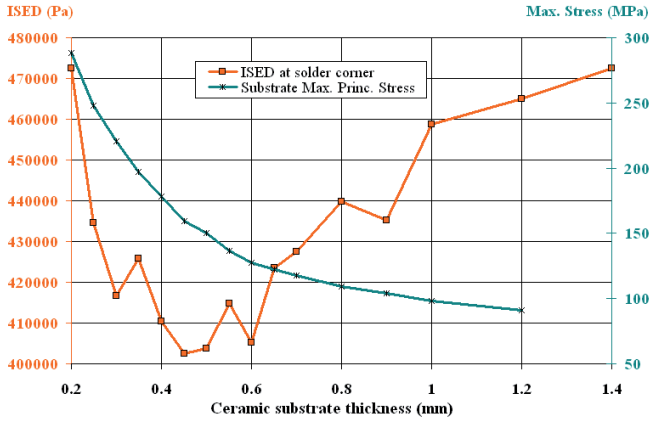

Fig. 26. Evolution of base plate solder corner ISED substrate maximal principal stress with substrate thickness.

while the thermal impedance increases linearly with a rate of about 0.013 K/(W mm). Regarding the base plate solder corner cyclic ISED, the simulations done here with a 300 μm copper metallized AlN substrate showed an optimum of substrate thickness between 0.4 and 0.6 mm. Additional simulations could be necessary for each specific application in order to determine the ceramic optimal thickness, with respect to the metallization material and thickness.

7 Conclusion

The objective of this study was to propose IGBT modules technologies based on materials available today, and propose design rules to optimise the lifetime for aeronautic applications. FEM based DoE was done with respect to the main failure modes under thermal and power cycling loading profiles.

This work showed that there was not optimal configuration of assembly (connection techniques, materials and dimensions) for all the applications, the designer should then take into account the most representative profile with the most critical design parameters to define the module. To do this, the results presented in this paper could be very helpful. It is obvious that complementary simulations could be necessary for each specific application in order to verify the interactions between all the parameters.

Five configurations are being manufactured for thermal and power cycling tests, in order to verify the predicted thermomechanical performances and failures criteria.

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