

The diagnostic research of telecom power converter with electromagnetic interference (EMI) suppressing technology

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Abstract – The main source of Electromagnetic Interference (EMI) emissions in power converters used for Telecom application comes from the high switching frequency of DC voltages. Power converters are generally operating in a periodic steady state, interested converter waveforms are typically periodic functions of time. Indeed the EMI emissions are a critical factor, which, can harm the system and degrade the satisfaction of Electromagnetic Compatibility (EMC). However, the most of design engineers use randomly various basic EMI reduction techniques. It is meaningful to quantify and analyze them before taking any solution measures. In fact, the diagnostic research of power converters is still under exploring. This article presents simplified equivalent circuit model used to predict the influence of common mode (CM) current noise in switching mode power supply. At the base of analysis, proposed equivalent circuit model contains essential couplings, parasitic elements, and sources occurred in the common mode current path. This circuit composed of input cables; equivalent voltage source and the intentional parameters of the converter is examined theoretically. A comparative analysis between practical results and the proposed model highlight good matching. At last, effective EMI suppressing techniques has been realized on an AC/DC converter prototype in order to validate the proposed model.

Key words: Diagnostic research; electro-magnetic interference (EMI); modelling and simulation.

1 Introduction

In recent years, with the growing number of electronic loads (computers, telecom, ...) and power supplies containing active devices at increased switching frequencies used to improve the efficiency and increase the power density, EMI noise is generated and propagates through the whole system (the supply and load) as can be seen in Figure 1. It can potentially harm the components or deteriorate the system's operation [1], then reduce the quality of both the input and output lines. Hence the existence of many standards [2] as EN55022, drive the study of minimizing and containing the conducted EMI. There are presently many techniques to reduce the EMI emissions of a power converter; some methods include, for example, passive and active filtering, shielding and grounding, noise balancing or cancelling, converter's controls, and packaging design [3–5]. Passive filtering is the most common method for EMI attenuation. With the inherent functionality of passive components the higher frequency characteristics become less ideal due to the parasitic, causing the attenuation of the EMI to decrease; in fact, it can

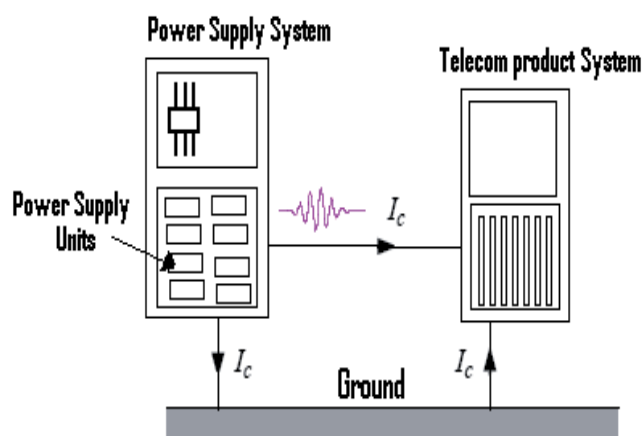


Fig. 1. Common Mode conducted emissions.

produce also other resonances in the conducted EMI frequency range. This causes the need for a second filter stage to attenuate at frequencies higher than the bandwidth of the first; in the radio frequency (RF) range. A variety of integrated EMI filters are proposed in [6] for this. However, it is not really the right choice, what can

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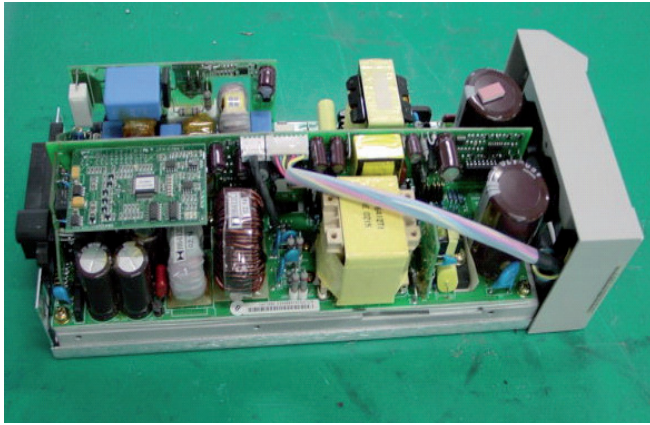


Fig. 2. Photo of actual AC/DC converter.

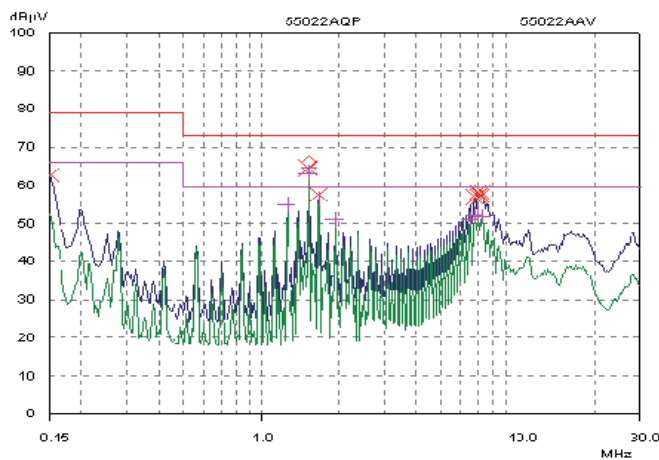


Fig. 3. Measured conducted EMI results from the input lines.

reduce drastically the cost, production time, and the reproducibility of a filter or layout design, is the need of analysing the EMI issues before randomly taking any solution process.

The purpose of this work is to propose a processing technique that will save the time and money spent on testing and redesigning the PCB layout of the converter without degrading the functionality of the filter.

In this paper, modelling method has been previously proposed in [7, 8] is verified with practical AC/DC. The conducted EMI standards limit (EN55022) is exceeded at resonance points 1.5 MHz and 7.5 MHz as can be seen in Figure 3. And in order to analyse these EMI peaks appeared in the common mode current path and ensure the correct choice of filters application, a simple equivalent circuit model is considered to simulate the resonance influence on common mode current. The circuit model is composed of parasitic parameters of the converter, capacitive couplings, inductive couplings, equivalent transient voltage source and the linear impedance stabilization network (LISN).

However, using this modelling approach, the switching mode power supply (SMPS) design engineer must have good understanding of the parasitic elements, the characteristics of components over a frequency range and the

PCB interconnections, which may cause the resonance point in the spectrum.

The bypassing technique traditionally applied for conducted common-mode noise reduction, is used to verify the validity of the circuit model.

2 Practical data

As shown in Figure 2 an actual AC/DC converter used for Telecom industry applications, consists of a PFC rectifier circuit with output voltage 400 V and switching frequency 50 kHz, followed by a DC/DC converter with output voltage 53 V and switching frequency 140 kHz. It was hypothesized that the DC/DC stage with high switching frequency would be the origin of the high common mode current measured due to a high dv/dt voltage transitions. Therefore, the voltage source used in the model is the actual transient voltage of the DC/DC converter. The conducted CM current noise measured at the input lines is shown in Figure 3. The resonant peak created near 7.5 MHz, is due to the capacitive coupling, which leads to increased common mode current picked up by the LISN. In addition, the EMI due to voltage-driven inductive coupling is very likely to exceed the limit at low frequency 1.5 MHz. This is occurred after earthing the output-positive cable, which resulted in resonance effect on common mode current generated in the victim loop lying just beyond the end of conductive emission limit.

3 Modelling of inductive and capacitive coupling

3.1 Capacitive coupling

In EMI Engineering, as in medical sciences, before deciding doing any sophisticated surgery; the Doctor must diagnose the case of the patient. Likewise before randomly taking any solution process, analysing the EMI issues is vital in achieving electromagnetic compatibility (EMC) compliance. However, using this modelling approach there is always a tension between accuracy and simplicity. Therefore, what is needed is an alternative simple circuit model based on the potential noise source and essential coupling paths. As shown in Figures 4a, 4b the equivalent circuit model is obtained by assuming that the common mode current (CM) is dominated by the following parasitic parameters: invisible capacitors to the earth creating capacitive coupling derived from the switching voltage nodes across the MOSFET's drain and source; LISN impedance terminals; input cables; earth; series parasitic elements LSR of output Y-capacitor where the common mode noise flow; PCB tracks and ground plane's inductances; and the converter parasitic impedance etc. This series combination of the parasitic parameters L_s and C_s in the common mode path consists of a parasitic resonant circuit, which can result in increased undesired resonant current detected by the LISN. Using the commercial OrCAD software program, as shown in Figure 5

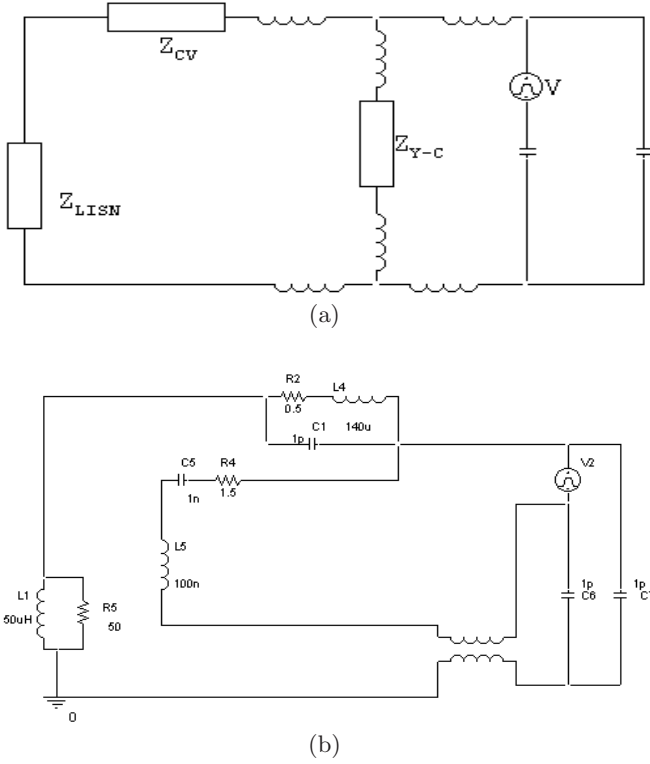


Fig. 4. The high frequency equivalent circuit model of the couplings for common mode currents. (a) Simplified equivalent circuit model of the couplings. (b) Equivalent circuit model with measured parameters values.

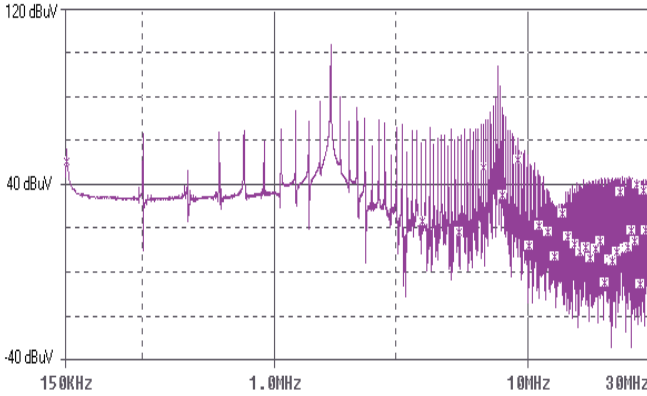


Fig. 5. Simulations of conducted EMI results from the input lines.

the simulation results demonstrate that the selected capacitive coupling path produces significant noise, which is picked up by the LISN at frequencies near the resonance peaks frequency 7.5 MHz. A conductor used as an interconnection is usually only part of a larger circuit, which contains a return path. The simulation results show that the stray capacitance between the high transient voltage conductor and a ground structure form part of a series resonant circuit with the inductance of the conductor. Thus the high current presenting a series resonance is the cause of the CM current peak at 7.5 MHz.

3.2 Inductive coupling

In an actual circuit, when the inductive coupling occurs, the source loop comprised of parasitic parameters of the converter and the LISN becomes a single primary winding of an air transformer, and the receptor loop becomes secondary. The simplified circuit model for combined inductive and capacitive couplings is shown in Figures 4a, 4b. The primary and secondary windings of a transformer resonate with the parasitic capacitances that appeared in the high frequency equivalent circuit, and which induce voltage down in the length of the receptor ground conductor and develop a current flow into the LISN terminals near the frequency 1.5 MHz as shown in Figure 5.

Interconnections also contain parasitic circuit elements, and the common mistake in an EMC/EMI evaluation is not to include the impedance of a conductor, especially when it is used to make a ground connection. In fact a conductor exhibits intrinsic or internal impedance comprised of an internal inductance (due to the internal magnetic flux), an external inductance (giving rise to an internal magnetic flux), an ac resistance, and a dc resistance. However, conductors invariably exhibit higher inductive reactance, due to external inductance, than does resistance even at low frequencies. The external inductance is often referred to as self-inductance and is usually higher than the internal inductance, when it is unintentional, as parasitic inductance. At a certain frequency the internal inductance begins to reduce by the square of the frequency. The external inductance is frequency independent [9, 10].

4 Parameters approximation and simulation results

In order to validate the simplified model without violating the physical meaning, realistic assumptions must be achieved. The stray capacitances to the earth and the inductance of tracks can be approximated using finite element analysis (FEA) software based on the physical data of the concerned conductors [11, 12]. The voltage induced in the loop victim is controlled by the mutual inductance M ; this mutual inductance depends on physical location of two loops, and is not easy to find because it is invisible. However, its value can be realistically estimated using the following equation [13]:

$$M = \mu_0 \left[\left(\frac{D}{2} \right) - \sqrt{\left(\frac{D}{2} \right)^2 - \left(\frac{d}{2} \right)^2} \right] H. \quad (1)$$

The above equation is to calculate the mutual inductance between a circular loop and the ground conductor, where D is the distance of the circle loop to the wire and d is the radius of the circle loop. The practically estimated value used in the simulation is $M = 9 \text{ uH}$.

The output Y-capacitor impedance is measured by using the impedance analyzer. Its parameters values are:

$$C_s = 1 \text{ nF}; \quad L_s = 100 \text{ nH}; \quad R_s = 1.5 \text{ } \Omega.$$

The conductor partial and total parasitic inductances can be either approximated using the FEA software or using the equations presented in [14]; in which the net inductance of a segment of loop is the sum of the self and mutual partial inductances of that segment. Each loop contains a total of N current segments and supporting a j current I_j . The total loop inductance L , in which the loop is broken into S segments, is typically approximated as $L = 500 \mu\text{H}$.

The remaining parasitic impedance in the circuit loop has also an inductive characteristic and its LSR equivalent elements are realistically estimated as the following:

$$L_s = 140 \mu\text{H}; \quad C_s = 1 \text{ pF}; \quad R_s = 0.5 \Omega.$$

5 Model validation

In order to absorb the conducted CM noise current produced by resonance, a parallel bypassing capacitor (with low impedance frequencies up to the point of self-resonance) is inserted in series with the damping resistor then shunted with the filtering output Y-capacitor, which connects the positive output line to the ground plane. Figures 6a, 6b shows an illustration of the actual converter and the high frequency equivalent circuit model. Thus, the insertion of such damping filter will reduce the first resonance pick at 1.5 MHz to under average limit as can be seen in Figure 7a, while the second resonance created near 7.5 MHz remains relatively unaffected because at frequencies above the self-resonance, bypassing performance is affected by other parasitic inductances present in the circuit [15]. However, by placing Y-capacitors C_y adjacent to LISN at the input lines location, the second resonance created near 7.5 MHz is also suppressed, since the impedance of this capacitance is very small at high frequencies and becomes lower than the LISN impedance 50Ω . Therefore, this prevents the additional common mode current caused by the second resonance from flowing trough LISN, and the most of CM current noise will flow trough the bypassing capacitor C_y and reduce the total CM noise picked up by the LISN. Figures 7a, 7b show the measured and simulation suppression results of both resonance picks appeared at the input lines.

6 Conclusion

In SMPS, unexpected increased current noise due to unexpected resonance. This results in a resonance peak that appears inside the conducted and radiated frequency range. The research results obtained are in good correlation between predicted conducted noise and measured values. Therefore, using a simplified lumped equivalent circuit model could be a viable method for forecasting and analysing EMI couplings and their effect in SMPS. Indeed, this modelling approach can help the design engineers to avoid the trial-and-errors. Alternatively, although not always effective, adding damping component in the

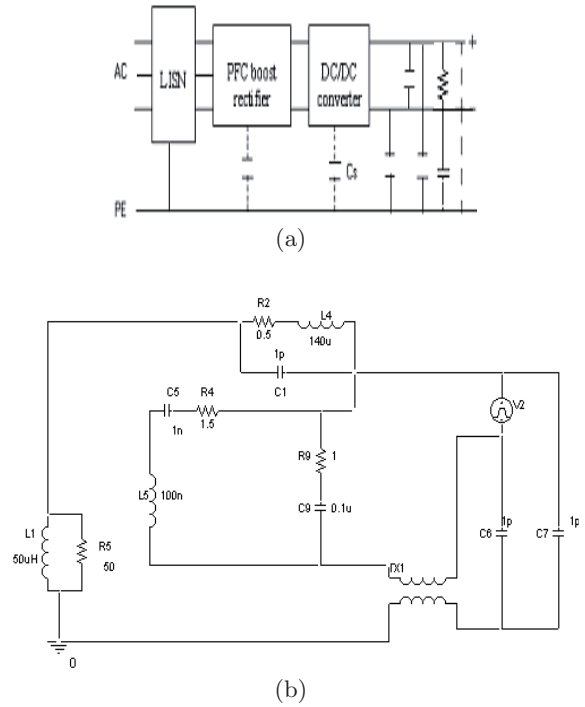


Fig. 6. Illustrations of the actual converter and the high frequency equivalent circuit model. (a) Actual circuit model. (b) Equivalent circuit model after adding damping components (RC).

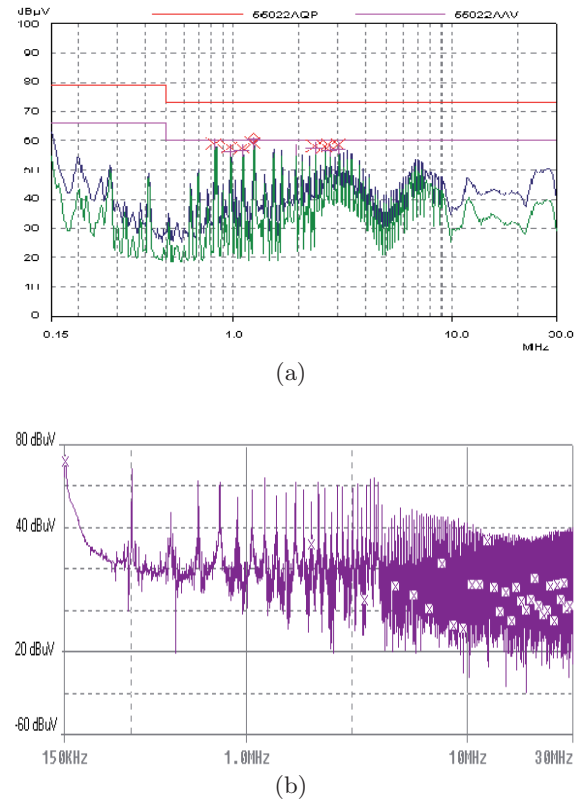


Fig. 7. Illustration of the second resonance pick suppression results from the input lines. (a) Measured conducted EMI results. (b) Simulation conducted EMI results.

resonating circuit path is usual practice to reduce resonance. In fact, it was used here in order only to verify the validity of the circuit model.

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